16PE713 FPGA Based System Design

Name: **SOLUTION** Reg. No: _____

Quiz #4 18th Jun 2018

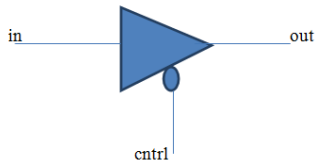
1. All ports by default are
   a) reg b) inout c) wires d) latches

2. Inout ports must always be
   a) reg b) trireg c) wires d) net

3. Which is used to introduce delays in circuit?
   a) Inverter b) xor gate c) buffer d) flip-flops

4. The left hand side of procedural continuous assignment can be
   a) Register or concatenation of registers b) Net or concatenation of nets
   c) Can be both registers or nets d) Array of registers

5. For the diagram given below choose the correct answer



   a) Propagate z if cntrl is asserted
   b) Propagate z if cntrl is deasserted
   c) Propagate 1 if cntrl is asserted
   d) Propagate 1 if cntrl is deasserted

6. Verilog HDL uses
   a) two-value logic b) four-value logic c) binary logic d) six-value logic

7. A model that describes the logic gates and the connections between logic gates in a design is
   a) switch-level b) gate-level c) data flow level d) behavioral level

8. Which of the following is not a primitive gate?
   a) and b) bufif0 c) mux d) nor

9. _____ is a basic which communicates externally through input, output, and bidirectional ports.
   a) module b) port c) nets d) registers

10. Complete the resolution table below for a 2-input NOR gate.

	0	1	X	Z
0	1	0	x	x
1	0	0	0	0
X	x	0	x	x
Z	x	0	x	x

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