Exp. No. Date:

FREQUENCY RESPONSE OF COMMON EMITTER AND COMMON COLLECTOR AMPLIFIERS

OBJECTIVE

The purpose of the experiment is to

design a single stage BJT common emitter (CE) amplifier with voltage divider biasing
explore the dc and ac characteristics of the CE amplifier
analyze and plot the frequency response of the amplifier with and without capacitor bypassed emitter resistance, also to compare the bandwidth of the amplifier with and without feedback.
design a common collector (CC) emitter follower circuit with voltage divider biasing network and to analyze the frequency response of a common collector amplifier

EQUIPMENT AND COMPONENTS USED

30 MHz Dual Channel Cathode Ray Oscilloscope

3 MHz Function Generator

0-30 V dc regulated power supply

4 ½ digit Digital Multimeter

Transistor BC107

Resistors ¼W

Electrolytic Capacitors

Breadboard and Connecting wires

BNC Cables and Probes

PRE-LAB

1. Read the specifications of BC107 transistor from its datasheet.

Device Part Number: BC107

Device Manufacturer: ______________________________

Maximum Collector to emitter voltage, V_{CEO} =

Maximum Emitter-base voltage , V_{EBO} =

Maximum Collector current, I_C =

Collector-Cut off Current, I_{CBO} =

DC current gain, h_{fe} =

Base Emitter Saturation Voltage, $V_{BE(Sat)}$ =

Collector Emitter Saturation Voltage, $V_{CE(sat)}$ =

Base Emitter On Voltage, $V_{BE(ON)}$ =

Input impedance, h_{ie} =

Reverse Voltage ratio, h_{re} =

Output admittance, h_{oe} =

Total power dissipation, P_{tot} =

2. Design a common emitter amplifier as per the design requirements given. With standard value of resistors, determine the dc operating conditions.

3. Comment on the mid-band gain and bandwidth of the CE amplifier with and without capacitor bypassed emitter resistance.

4. Comment on the mid-band gain and bandwidth of the common collector amplifier.

CIRCUIT DIAGRAM

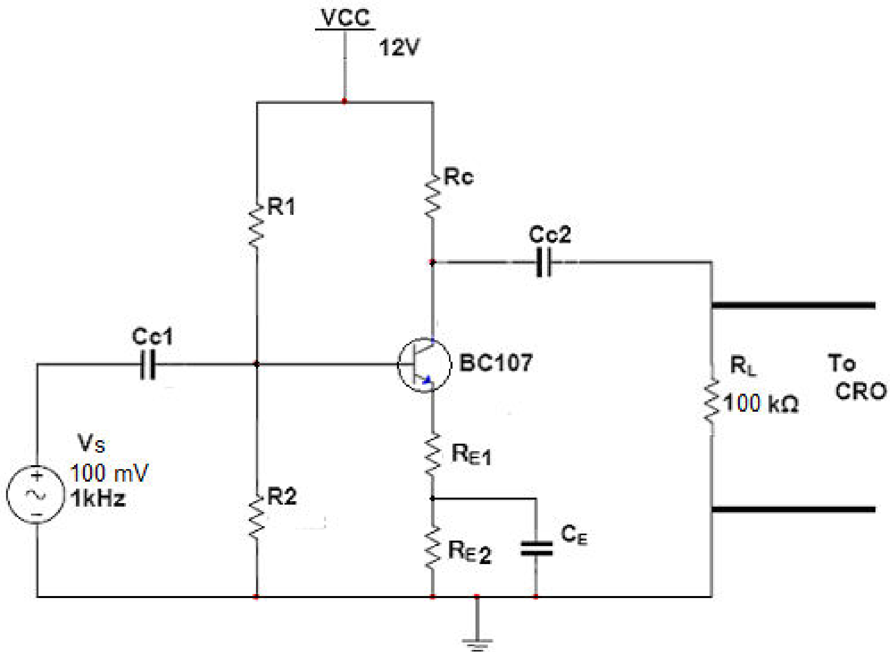

Figure1. Common Emitter Amplifier

DESIGN

Output requirements: Mid-band voltage gain of the amplifier, A_V = 50 V/V

Select the general purpose transistor BC107.

Specifications of BC107

Type: NPN

Nominal ratings: V_{CE} = 5 V, I_C=2 mA, h_{FE}=110 to 450

DC biasing conditions V_{CC}=12 V, I_C=5 mA

V_{RC}=40% of V_{CC} =

V_{RE}=10% of V_{CC} =

V_{CEQ}=50% of V_{CC} =

Design of Collector resistor R_C

$V_{RC} = I_C \times R_C$

=> $V_{CEQ} = V_{CC} - V_{RC}$

=> $V_{RC} = V_{CC} - V_{CEQ}$

=> $R_C = (V_{CC} - V_{CEQ}) / I_C$ =

Design of Emitter resistor R_E

$V_{RE} = I_E \times R_E$

=> R_E =

Design of voltage divider R_1 and R_2

$I_B = I_C/h_{FE}$ Take h_{FE} = 200

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Assume current through R_1=10 I_B and that through R_2=9 I_B to avoid loading the potential divider network R_1 and R_2 by the base current.

V_{R2} = voltage across R_2 = V_{BE} + V_{RE} =

Also $V_{R2} = 9I_BR_2$ =

Then R_2 =

V_{R1} = voltage across R_1 = $V_{CC} - V_{R2}$ =

Also $V_{R1}=10I_BR_1$ =

Then R_1 =

Design of Load R_L

Take R_L = 100 kΩ

Design of unbiased emitter resistor

$g_m = I_C / V_T$ = (Take V_T = 0.026 V)

$$A_v = \frac{-g_m * R_c}{g_m * R_{E1} + 1}$$

R_{E1} =

$R_E = R_{E1} + R_{E2}$ => $R_{E2} = R_E - R_{E1}$ =

Design of coupling capacitors C_{C1} and C_{C2}

$X_{C1} \leq$ Rin/10.

Here $R_{in} = R_1 \parallel R_2$

Rin =

Then $X_{C1} \leq$

So $C_{C1} \geq 1/2\pi f \times X_{C1}$ =

$X_{C2} \leq$ Rout/10, where Rout = Rc.

Then $X_{C2} \leq$

$C_{C2} \geq 1/2\pi f \times X_{C2}$ =

Design of bypass capacitors C_E

To bypass the lowest frequency (say 100 Hz), X_{CE} should be equal to one-tenth or less than the resistance R_E.

$X_{CE} \leq R_E/10$

$C_E \geq 1/2\pi \times 100 \times X_{CE}$ =

PRACTICE PROCEDURE

1. COMMON EMITTER AMPLIFIER

DC Operating Point

1. Connect the voltage divider bias network from the circuit shown in Figure 1.
2. Apply DC bias voltage V_{CC} and measure the operating point quantities: V_B, V_{BE}, V_C, V_{CE}, V_{RE}, I_C.

Table1: Operating Point measurements

Quantities	Measured Value	Designed Value
Base Voltage, V_B		
Base-emitter voltage, V_{BE}		
Collector Voltage, V_C		
Collector–emitter voltage, V_{CE}		
Collector Current, I_C		
Emitter Voltage, V_{RE}		

Inference

Amplifier Gain Measurements

1. Connect the circuit as shown in Figure 1.
2. Apply an input sine wave signal of 100mV, 1 kHz from the function generator.
3. Observe the output in CRO. Calculate the corresponding gain and compare with the designed values.

Table2: Amplifier gain measurements

	Amplitude (V)	Time Period (ms)	Frequency (kHz)	Voltage gain, A_V (V/V)
Small signal Input voltage, Vs				
Amplified output voltage, Vo with bypass capacitor				
Amplified output voltage, Vo without bypass capacitor				

Inference

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Frequency Response

1. Keeping the magnitude of the input same, ie.,100mV, vary the frequency of the input signal and tabulate the output voltage for different frequencies.
2. Compute the gain and plot the Frequency versus Gain (dB) using semi-log sheet.
3. From the plot, determine the values of (a) Mid band voltage gain, A_V(mid), (b) Lower cut-off frequency, (c) Upper cut-off frequency and (d) Bandwidth.

Repeat the above by removing the bypass capacitor.

Table3: Frequency response with bypass capacitor

Input voltage, Vs = mV

Signal frequency (Hz)	Output voltage, Vo (Volts)	Gain = $\frac{V_o}{V_S}$	20 $\log_{10}$(Gain) dB
10			
20			
50			
100			
200			
500			
1k			
2k			
5k			
10k			
20k			
50k			
100k			
200k			
500k			
1M			

Inference

Table4: Frequency response without bypass capacitor

nput voltage, Vs = mV

Signal frequency (Hz)	Output voltage, Vo (volts)	Gain = $\frac{Vo}{Vs}$	20 $\log_{10}$(Gain) dB
10			
20			
50			
100			
200			
500			
1k			
2k			
5k			
10k			
20k			
50k			
100k			
200k			
500k			
1M			

Inference

2. COMMON COLLECTOR AMPLIFIER

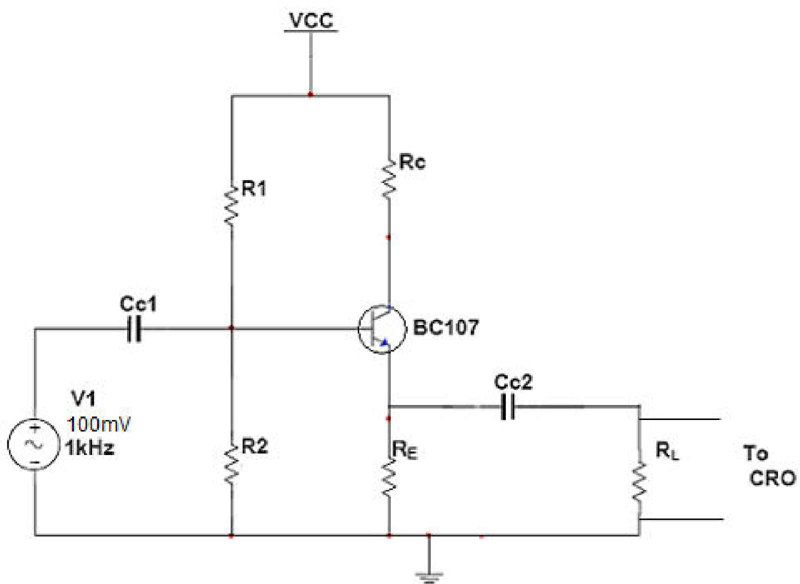

Figure2. Common Collector Amplifier

Amplifier Gain Measurements

1. Connect the circuit as shown in Figure 2.
2. Apply an input sine wave signal of 100mV, 1 kHz from the function generator.
3. Observe the output in CRO. Calculate the corresponding gain and compare with the designed values.

Table1: Amplifier gain measurements

	Amplitude (V)	Time Period (ms)	Frequency (kHz)
Small signal Input voltage, Vs			
Amplified output voltage, Vo			

Voltage gain, A_V =

Inference

Frequency Response

1. Keeping the magnitude of the input same, ie.,100mV, vary the frequency of the input signal and tabulate the output voltage for different frequencies.
2. Compute the gain and plot the Frequency versus Gain (dB) using semi-log sheet.
3. From the plot, determine the values of (a) Mid band voltage gain, A_V(mid), (b) Lower cut-off frequency, (c) Upper cut-off frequency and (d) Bandwidth.

Table2: Frequency response of CC amplifier

Input voltage, Vi = mV

Signal frequency (Hz)	Output voltage, Vo (Volts)	Gain = $\frac{V_o}{V_i}$	20 $\log_{10}$(Gain) dB
10			
20			
50			
100			
200			
500			
1k			
2k			
5k			
10k			
20k			
50k			
100k			
200k			
500k			
1M			

Inference

UNDERSTANDING & LEARNING

RESULTS AND CONCLUSION

Prepared by:

Name: ______________________________ Reg. No.: ____________________

Date of Experiment: ……………

Date of Report Submission: ……………

Signature

ASSESSMENT

Student Task	Max. Marks	Graded Marks
Pre-lab Preparation / Conduction	10	
Results & Inference	10	
Post-lab / Viva-voce	10	
Total	30	