Exp. No. Date:

FREQUENCY RESPONSE OF COMMON SOURCE AMPLIFIER

OBJECTIVE

The purpose of the experiment is to

design a single stage MOSFET common source (CS) amplifier with voltage divider biasing

analyze and plot the frequency response of the amplifier with and without capacitor bypassed source resistance, also to compare the bandwidth of the amplifier with and without feedback.

EQUIPMENT AND COMPONENTS USED

30 MHz Dual Channel Cathode Ray Oscilloscope
3 MHz Function Generator
0-30 V dc regulated power supply
4 ½ digit Digital Multimeter
MOSFET 2N7000
Resistors ¼W
Electrolytic Capacitors
Breadboard and Connecting wires
BNC Cables and Probes

PRE-LAB

1. Read the specifications of 2N7000 transistor from its datasheet.
   Device Part Number: 2N7000
   Device Manufacturer: _____
   Drain – source voltage, V_{DS} =
   Gate-source voltage, V_{GS} =
   Drain Current, I_D =
   Gate Threshold Voltage, $V_{GS(th)}$ =
   Drain−Source Breakdown Voltage, $V_{(BR)DSS}$ =
   Static Drain−Source On Resistance, $r_{DS(ON)}$ =

2. Design a common source amplifier as per the design requirements given. With standard value of resistors, determine the dc operating conditions.

3. Comment on the mid-band gain and bandwidth of the CS amplifier with and without capacitor bypassed source resistance.

CIRCUIT DIAGRAM

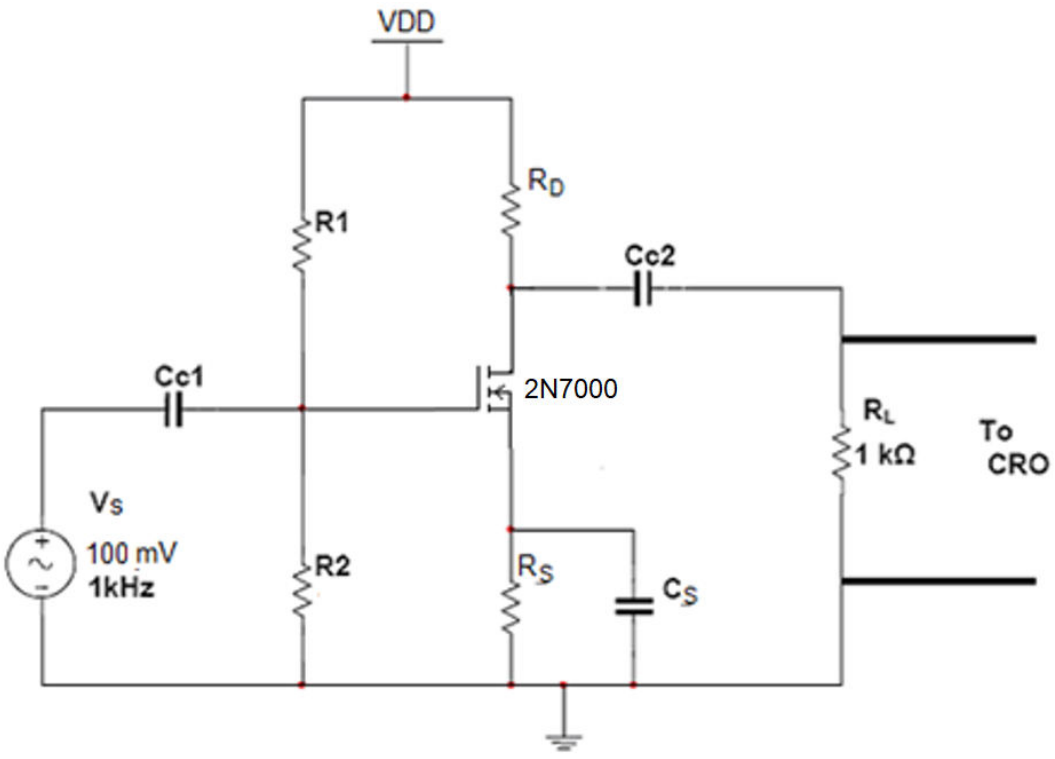

Figure1. Common Source Amplifier

DESIGN

Output requirements: Mid-band voltage gain of the amplifier, A_V = 50 V/V

Select the MOSFET as 2N7000.

DC biasing conditions

V_{DD}=12 V, I_D=5 mA

V_{RD}=45% of V_{DD} =

V_{RS}=10% of V_{DD} =

V_{DS}=45% of V_{DD} =

Design of Drain resistor R_D

$V_{RD} = I_D \times R_D$

=> R_D =

Design of Source resistor R_S

$V_{RS} = I_D \times R_S$, here $I_S = I_D$

=> R_S =

Design of voltage divider R_1 and R_2

Take V_{GS} = 2.5 V (above Vt, in saturation region)

$V_{GS} = V_G - V_S$ => $V_G = V_{GS} + V_S$ =

Use large value for R_1 to ensure zero gate current. Take R_1 = 240 kΩ

$V_{R2} = V_G = V_{DD} \left(\frac{R2}{R1+R2}\right)$

Then R_2 =

Design of Load Resistor, R_L

$A_V = g_m(R_D||R_L)$

Take g_m = 50 mS, R_L =

Design of blocking capacitors C_{C1} and C_{C2}

Impedance of the coupling capacitor $X_C \leq R_G/10$

Using f_L=100Hz, $C_{C1} \geq 1/(2\pi f \times X_{C1})$ =

$C_{C1} = C_{C2}$ =

Design of bypass capacitor

Take $X_{CS} \leq R_S/10$ at 100Hz to bypass this frequency

$C_S \geq 1/2\pi \times 100 \times X_{CS}$

C_S =

PRACTICE PROCEDURE

DC Operating Point

1. Connect the voltage divider bias network from the circuit shown in Figure 1.
2. Apply DC bias voltage V_{DD} and measure the operating point quantities: V_{GS}, V_{DS}, I_D.

Table1: Operating Point measurements

Quantities	Designed Value	Measured Value
Gate-source Voltage, V_{GS}		
Drain-Source Voltage, V_{DS}		
Drain Current, I_D		

Inference

Amplifier Gain Measurements

1. Connect the circuit as shown in Figure 1.
2. Apply an input sine wave signal of 100mV, 1 kHz from the function generator.
3. Observe the output in CRO. Calculate the corresponding gain.

Table2: Amplifier gain measurements

	Amplitude (V)	Frequency (kHz)	Voltage gain, A_V (V/V)
Small signal Input voltage, Vs			
Amplified output voltage, Vo with bypass capacitor			
Amplified output voltage, Vo without bypass capacitor			

Inference

Frequency Response

1. Keeping the magnitude of the input same, ie.,100mV, vary the frequency of the input signal and tabulate the output voltage for different frequencies.
2. Compute the gain and plot the Frequency versus Gain (dB) using semi-log sheet.
3. From the plot, determine the values of (a) Mid band voltage gain, A_V(mid), (b) Lower cut-off frequency, (c) Upper cut-off frequency and (d) Bandwidth.

Repeat the above by removing the bypass capacitor.

Table3: Frequency response with bypass capacitor

Input voltage, Vs = mV

Signal frequency (Hz)	Output voltage, Vo (Volts)	Gain = $\frac{Vo}{V_S}$	20 $\log_{10}$(Gain) dB
10			
20			
50			
100			
200			
500			
1k			
2k			
5k			
10k			
20k			
50k			
100k			
200k			
500k			
1M			

Inference

Table4: Frequency response without bypass capacitor

input voltage, Vs = mV

Signal frequency (Hz)	Output voltage, Vo (volts)	Gain = $\frac{Vo}{Vs}$	20 $\log_{10}$(Gain) dB
10			
20			
50			
100			
200			
500			
1k			
2k			
5k			
10k			
20k			
50k			
100k			
200k			
500k			
1M			

Inference

UNDERSTANDING & LEARNING

RESULTS AND CONCLUSION

Prepared by:
Name: _____ Reg. No.: _____

Date of Experiment: ……

Date of Report Submission: ……

Signature

ASSESSMENT

Student Task	Max. Marks	Graded Marks
Pre-lab Preparation / Conduction	10	
Results & Inference	10	
Post-lab / Viva-voce	10	
Total	30	