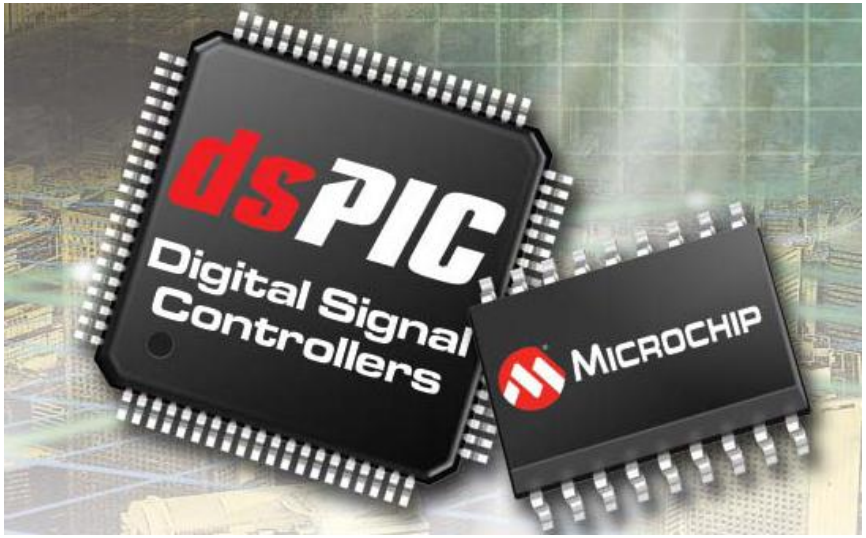
EE427 Advanced Microcontrollers

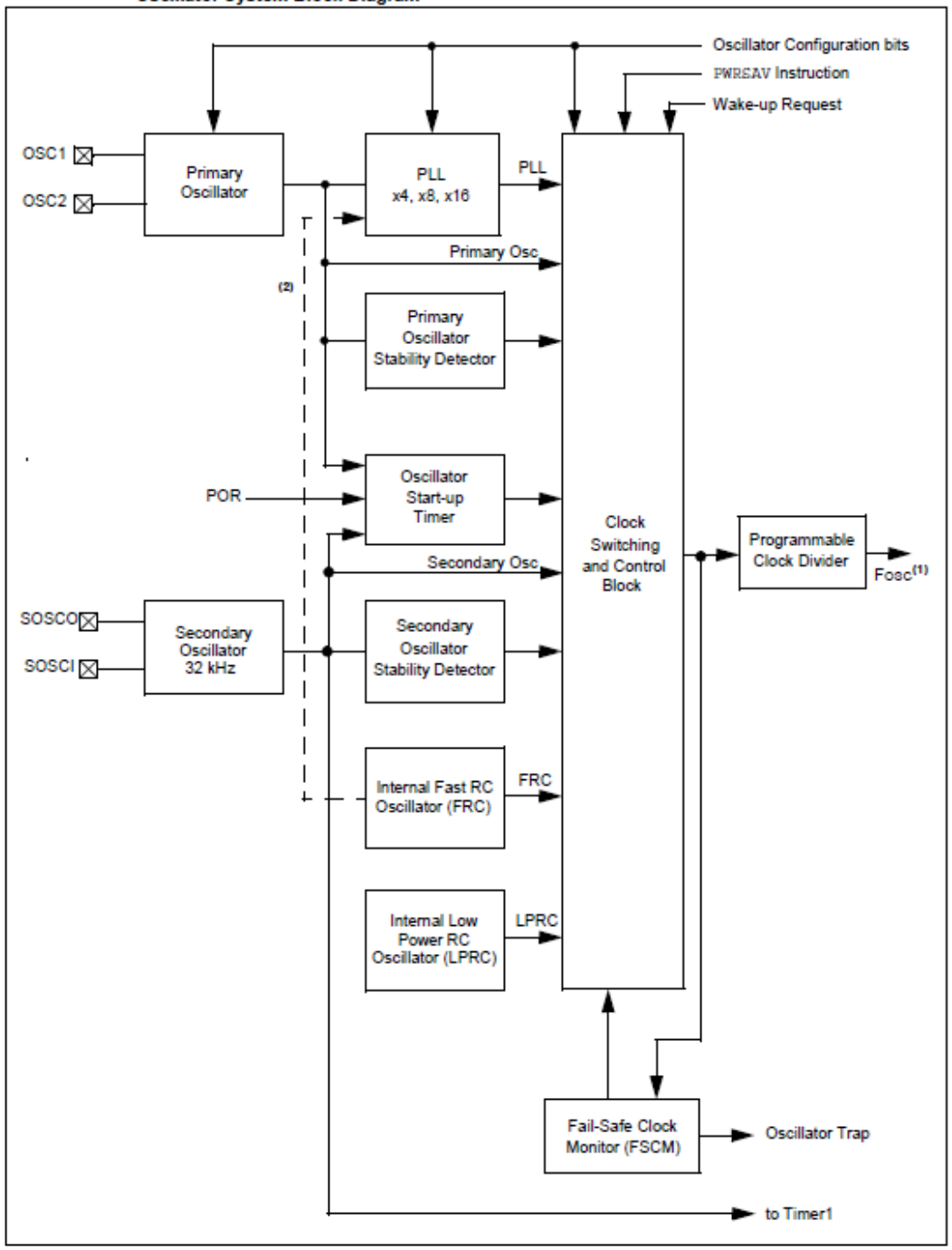


Oscillators

Oscillator System

- oscillator system has the following modules and features:
  - Various external and internal oscillator options as clock sources
  - An on-chip PLL to boost internal operating frequency
  - Clock switching between various clock sources
  - Programmable clock postscaler for system power savings
  - A Fail-Safe Clock Monitor (FSCM) that detects clock failure and takes fail-safe measures

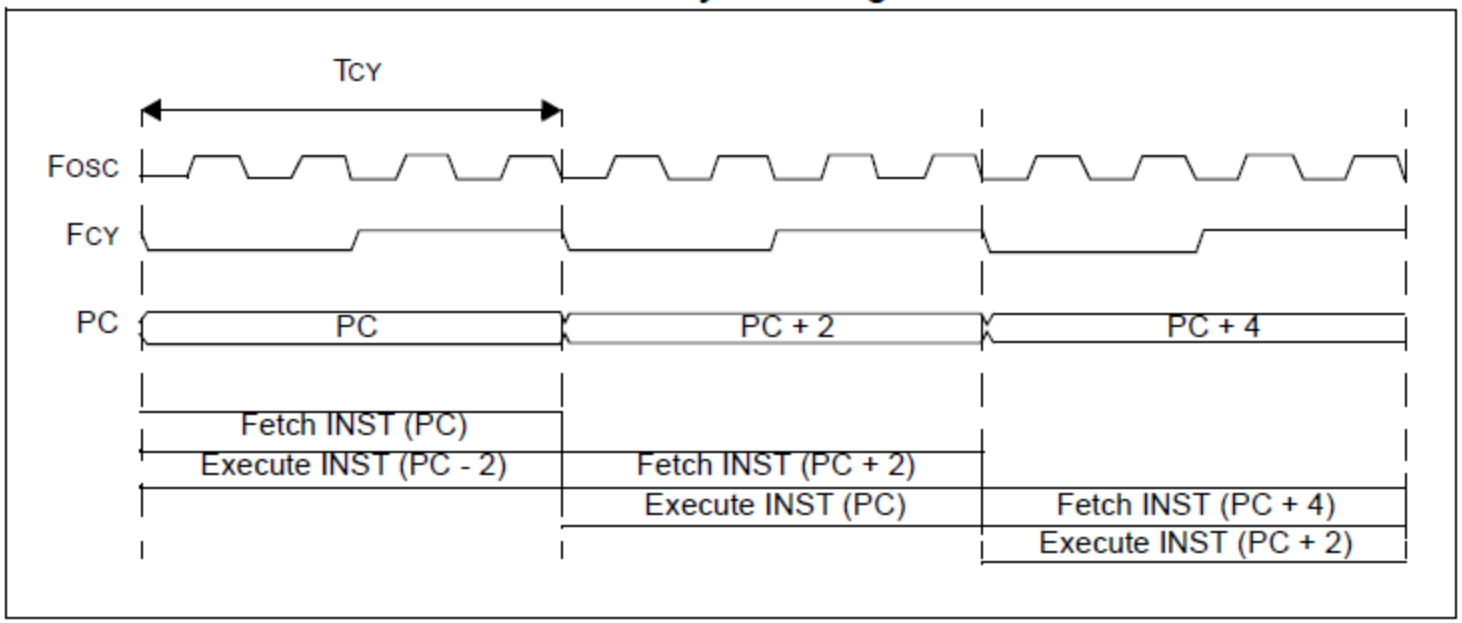
Oscillator System Block Diagram



Device Clocking

- system clock source can be provided by one of four sources:
  - Primary oscillator
  - Secondary oscillator
  - Internal Fast RC (FRC) oscillator
  - Low-Power RC (LPRC) oscillator
- The system clock source is divided by four to produce the internal instruction cycle clock, F_{CY}. In
- this document, the instruction cycle clock is also denoted by $F_{OSC}/4$.

Clock/Instruction Cycle Timing



$$FCY = \frac{FOSC}{4} = \left(\frac{\text{SOURCE OSCILLATOR FREQUENCY} * \text{PLL MULTIPLIER}}{\text{PROGRAMMABLE POSTSCALER} * 4}\right)$$

Primary Oscillator

- Primary oscillator is available on the OSC1 and OSC2 pins of the dsPIC30F device family.
- has a wide variety of operation modes with frequency ranging from 32kHz to 40MHz.
- can be configured for an external clock input, external RC network, or an external crystal.

Secondary Oscillator

- The Low Power(LP) or Secondary oscillator is designed specifically for low power operation with a 32 kHz crystal.
- serves as a secondary crystal clock source for low power operation.
- LP oscillator can also drive Timer1 for a real-time clock application.

Internal Fast RC Oscillator (FRC)

- The FRC oscillator is a fast (7.37 MHz nominal) internal RC oscillator.

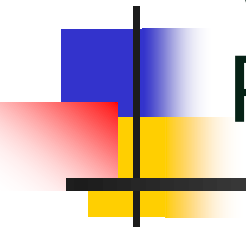
- This oscillator is intended to provide a range of device operating speeds without the use of an external crystal, ceramic resonator or RC network.

Internal Low-Power RC (LPRC) Oscillator

- The LPRC oscillator is a component of the Watchdog Timer (WDT)
- oscillates at a nominal frequency of 512 kHz.

- LPRC oscillator is the clock source for the Power-up Timer (PWRT) circuit, WDT and clock monitor circuits.

- It may also be used to provide a low frequency clock source option for applications where power consumption is critical, and timing accuracy is not required.



Watchdog Timer (WDT) and Power Saving modules

Power Saving Modes

- dsPIC DSC devices have two reduced Power modes that can be entered through execution of the `PWRSAV` instruction
  - Sleep Mode
  - Idle Mode

- Sleep Mode: CPU, system clock source, and any peripherals that operate on the system clock source are disabled. This is the lowest Power mode for the device.
  - **`PWRSAV #SLEEP_MODE`**

Power Saving Modes

- Idle Mode: The CPU is disabled, but the system clock source continues to operate.
- Peripherals continue to operate, but can optionally be disabled.
  - **`PWRSAV #IDLE_MODE`**
- The Power Saving modes can be exited as a result of an enabled interrupt, WDT time-out, or a device Reset.
- When the device exits one of these two Operating modes, it is said to ‘wake-up’.

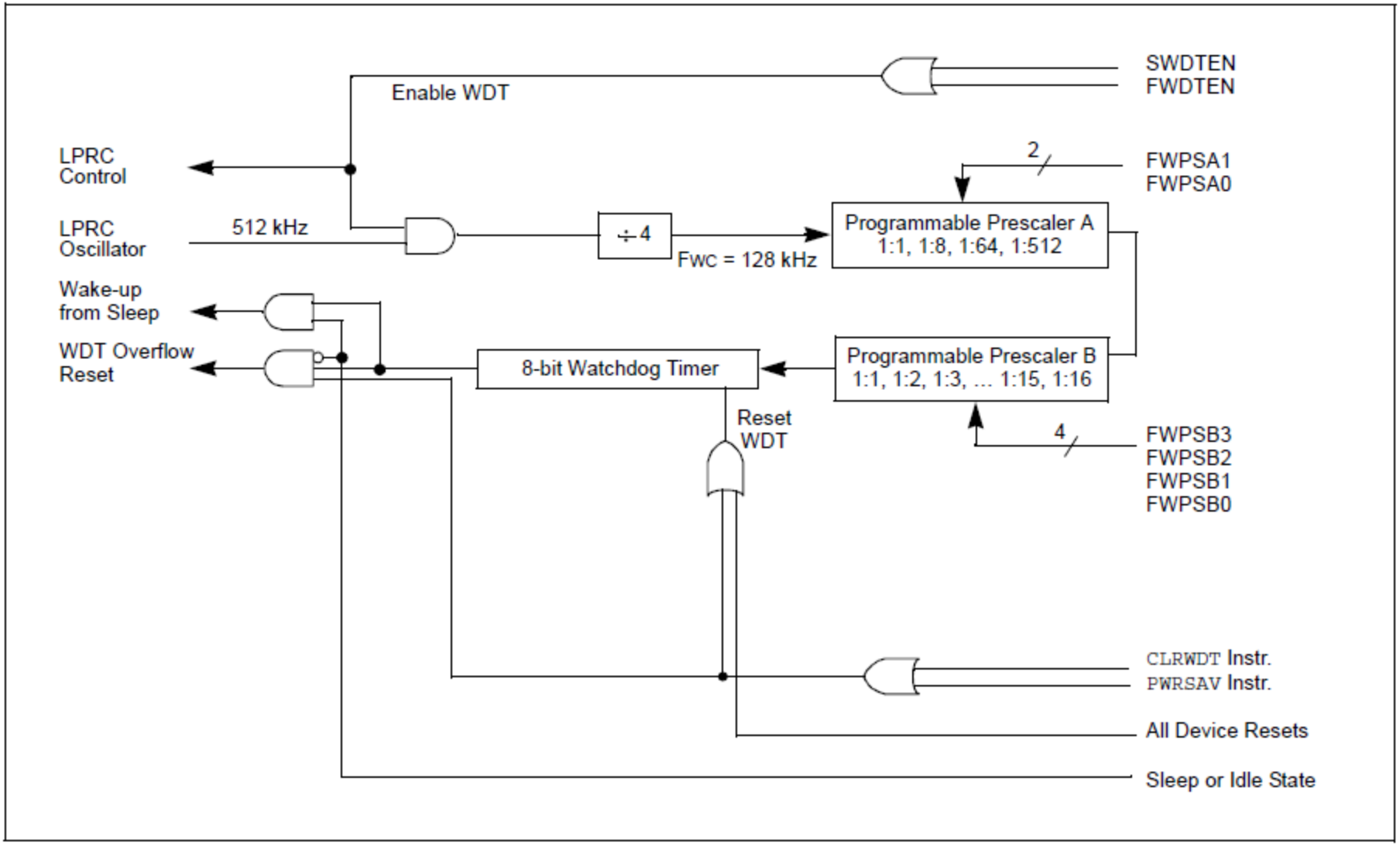
- The processor will exit, or ‘wake-up’, from Sleep on one of the following events:
  - On any interrupt source that is individually enabled
  - On any form of device Reset
  - On a WDT time-out

- The processor will wake from Idle mode on the following events:
  - On any interrupt that is individually enabled.
  - On any source of device Reset.
  - On a WDT time-out.

Watchdog Timer

- Primary function of the Watchdog Timer (WDT) is to reset the processor in the event of a software malfunction.
- WDT is a free running timer, which runs on the internal LPRC oscillator requiring no external components.
- WDT timer will continue to operate even if the system clock source (e.g., the crystal oscillator) fails.

WDT Block Diagram



WDT Prescalers

- The WDT has two clock prescalers to allow a wide variety of time-out periods
  - Prescaler A
  - Prescaler B,
- Prescaler A can be configured for **1:1**, **1:8**, **1:64** or **1:512** divide ratios.
- Prescaler B can be configured for any divide ratio from **1:1** through **1:16**.
- Time-out periods range between 2 ms and 16 seconds (nominal) using the prescalers

  - **WDT Period = 2 ms x Prescale A x Prescale B**

WDT Time-out Period vs. Prescale A and Prescale B Settings

Prescaler B Value	Prescaler A Value			
	1	8	64	512
1	2	16	128	1024
2	4	32	256	2048
3	6	48	384	3072
4	8	64	512	4096
5	10	80	640	5120
6	12	96	768	6144
7	14	112	896	7168
8	16	128	1024	8192
9	18	144	1152	9216
10	20	160	1280	10240
11	22	176	1408	11264
12	24	192	1536	12288
13	26	208	1664	13312
14	28	224	1792	14336
15	30	240	1920	15360
16	32	256	2048	16384

Note: All time values are in milliseconds.

Peripheral Module Disable (PMD) Registers

- Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module.

- When a peripheral is disabled via the appropriate PMD control bit, the peripheral is in a minimum power consumption state.

- The control and status registers associated with the peripheral will also be disabled so writes to those registers will have no effect and read values will be invalid.

Peripheral Module Disable (PMD) Registers

- If a PMD bit is set, the corresponding module is disabled after a delay of 1 instruction cycle.

- If a PMD bit is cleared, the corresponding module is enabled after a delay of 1 instruction cycle