EE427 Advanced Microcontrollers

DSP Instructions

Multi-cycle Instructions

- Most of dsPIC instructions execute in single cycle, with the following exceptions:
  - `DO`
  - `LNK, ULNK`
  - `MOV.D, PUSH.D`
  - `TBLRDH, TBLRDL, TBLWTH, TBLWTL` and
  - instructions that change the program counter
- These instructions require 2 cycles to execute
- Instructions `DIV.S, DIV.U` and `DIVF` are single-cycle instructions, which should be executed 18 consecutive times as the target of a `REPEAT` instruction

Multi-cycle Instructions

- `RETFIE, RETLW` and `RETURN` are a special case of an instruction that changes the program counter.
- These execute in 3 cycles

Multi-Word Instructions

- `CALL, DO` and `GOTO` instructions, which are Program Flow Instructions, require two words of memory as their opcodes embed large literal operands

DSP MAC Instructions

- DSP MAC instructions utilize both the X and Y data paths of the CPU core, Which enables these instructions to perform the following operations all in one cycle:
  - two reads from data memory using prefetch working registers (MAC Prefetches)
  - two updates to prefetch working registers (MAC Prefetch Register Updates)
  - one mathematical operation with an accumulator (MAC Operations)

DSP MAC Instructions

Instruction	Description
CLR	Clear accumulator
ED	Euclidean distance (no accumulate)
EDAC	Euclidean distance
MAC	Multiply and accumulate
MAC	Square and accumulate
MOVSAC	Move from X and Y bus
MPY	Multiply to accumulator
MPY	Square to accumulator
MPY.N	Negative multiply to accumulator
MSC	Multiply and subtract

MAC Operations

- The mathematical operations performed by the MAC class of DSP instructions multiply the contents of two working registers and either add or store the result to either Accumulator A or Accumulator B.
- This is the operation of the MAC, MPY, MPY.N and MSC instructions.

Base MAC Syntax

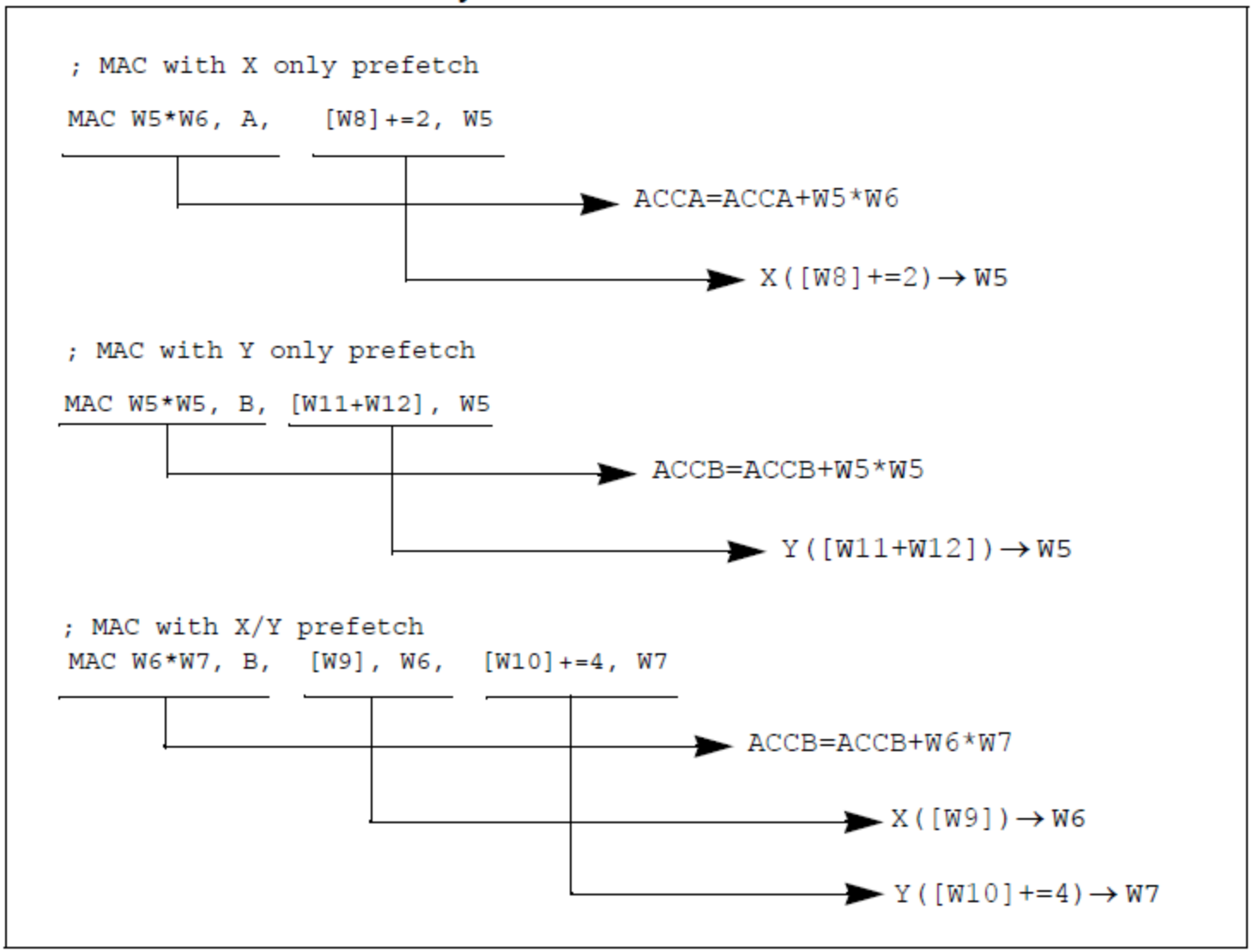
```
; MAC with no prefetch
MAC W4*W5, A
```

→ Multiply W4*W5, Accumulate to ACCA

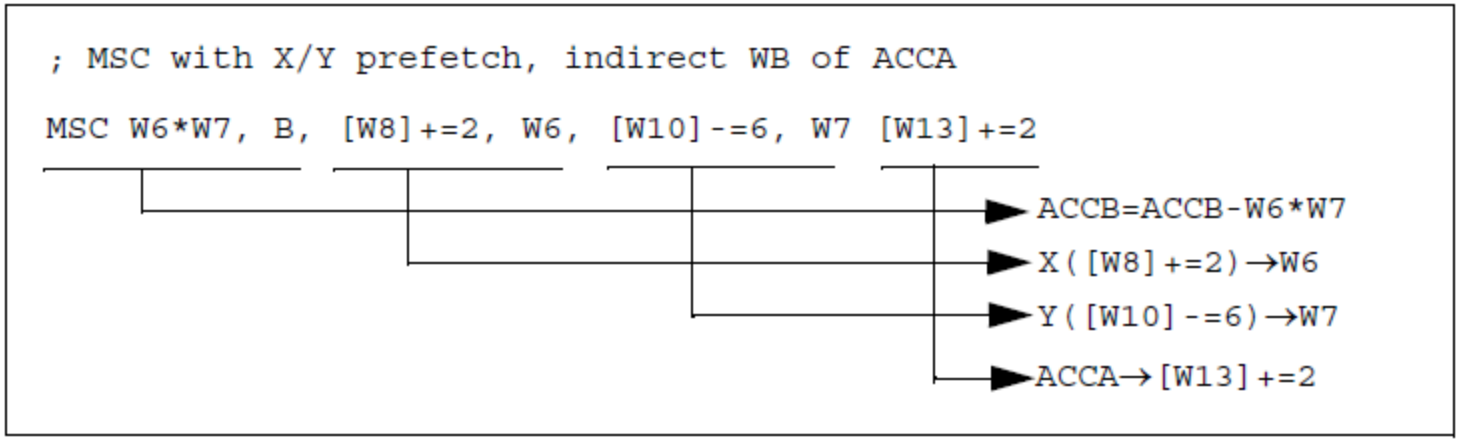
```
; MAC with no prefetch
MAC W7*W7, B
```

→ Multiply W7*W7, Accumulate to ACCB

MAC Prefetch Syntax



MSC Instruction with Two Prefetches and Accumulator Write Back



DSP Accumulator Instructions

- The DSP Accumulator instructions do not have prefetch or accumulator WB ability, but they do provide the ability to add, negate, shift, load and store the contents of either 40-bit Accumulator.
- `ADD` and `SUB` instructions allow the two accumulators to be added or subtracted from each other.

DSP Accumulator Instructions

Instruction	Description
ADD	Add accumulators
ADD	16-bit signed accumulator add
LAC	Load accumulator
NEG	Negate accumulator
SAC	Store accumulator
SAC.R	Store rounded accumulator
SFTAC	Arithmetic shift accumulator by Literal
SFTAC	Arithmetic shift accumulator by (Wn)
SUB	Subtract accumulators