Exp. No #5 Date:

FREQUENCY RESPONSE OF COMMON COLLECTOR AMPLIFIER

OBJECTIVE

The purpose of the experiment is to analyze and plot the frequency response of a common collector amplifier.

EQUIPMENT AND COMPONENTS USED

30 MHz Dual Channel Cathode Ray Oscilloscope
3 MHz Function Generator
0-30 V dc dual regulated power supply
4 ½ digit Digital Multimeter
Transistor BC107
47kΩ, 10kΩ, 2.2kΩ, 680Ω, 1kΩ Resistors, ¼ W
10μF, 15μF Electrolytic capacitors
Breadboard and Connecting wires
BNC Cables and Probes

THEORY

- In common collector amplifier, the external load is capacitor-coupled to the transistor emitter terminal.
- The important feature of common collector amplifier is that, its input resistance is very large and output resistance is small compared to other configurations. Its voltage gain is close to unity.
- There is no phase inversion between the input and output.
- Common collector amplifier is called as emitter follower as the phase of the output signal at emitter follows the phase of the input signal at base.
- CC amplifiers are used for impedance matching applications

FURTHER READING

1. Robert Boylstad, Louis Nashelsky, “Electronic Devices and Circuit Theory”, PHI, 2008.
2. James Cox, ‘Fundamentals of Linear Electronics: Integrated and Discrete’, Delmar Thomson Learning, 2nd edition, 2001.
3. Theodore F.Bogart, Jeffrey S.Beasley, “Electron Devices and Circuits, PHI.
4. Robert Diffenderfer, “Electronic Devices”, Delmar Cengage Learning, 2005.

PRELAB

1. Use SPICE to create a common collector amplifier. Observe the dc operating conditions.

2. Obtain a plot of the frequency response of the common collector amplifier over the frequency range from 1 Hz through 1 MHz. Observe the gain and bandwidth.

3. [Optional] Determine the input impedance and output impedance of the amplifier.

DESIGN

Select the general purpose transistor BC107.

Specifications of BC107

Type: NPN

Nominal ratings: V_{CB} = 5 V, I_C=2 mA, h_{FE}=100 to 500

DC biasing conditions V_{CC}=12 V, I_C=2 mA

V_{RC}=40% of V_{CC} =

V_{RE}=10% of V_{CC} =

V_{CE}=50% of V_{CC} =

Design of Collector resistor R_C

$V_{RC} = I_C \times R_C$

$\Rightarrow R_C =$

Design of Emitter resistor R_E

$V_{RE} = I_E \times R_E$, here $I_E = I_C$

$\Rightarrow R_E =$

Design of voltage divider R_1 and R_2

$I_B=I_C/h_{FE}$ (choose h_{FE} = 100)

=

Assume current through R_1=10 I_B and that through R_2=9 I_B to avoid loading the potential divider network R_1 and R_2 by the base current.

V_{R2} = voltage across R_2 = V_{BE} + V_{RE} =

Also $VR_2 = 9I_BR_2$ =

Then R_2 =

V_{R1} = voltage across R_1 = V_{CC} – V_{R2} =

Also $VR_1=10I_BR_1$ =

Then R_1 =

Design of Load R_L

Assume R_L = 1 kΩ

Design of coupling capacitors C_{C1} and C_{C2}

$X_{C1} \leq Rin/10$.

Here $R_{in} = R_1$ II R_2

Rin =

Then $X_{C1} \leq$

So $C_{C1} \geq 1/2\pi f \times X_{C1}$ =

$X_{C2} \leq Rout/10$, where Rout = Rc.

Then $X_{C2} \leq$

$C_{C2} \geq 1/2\pi f \times X_{C2}$ =

CIRCUIT DIAGRAM

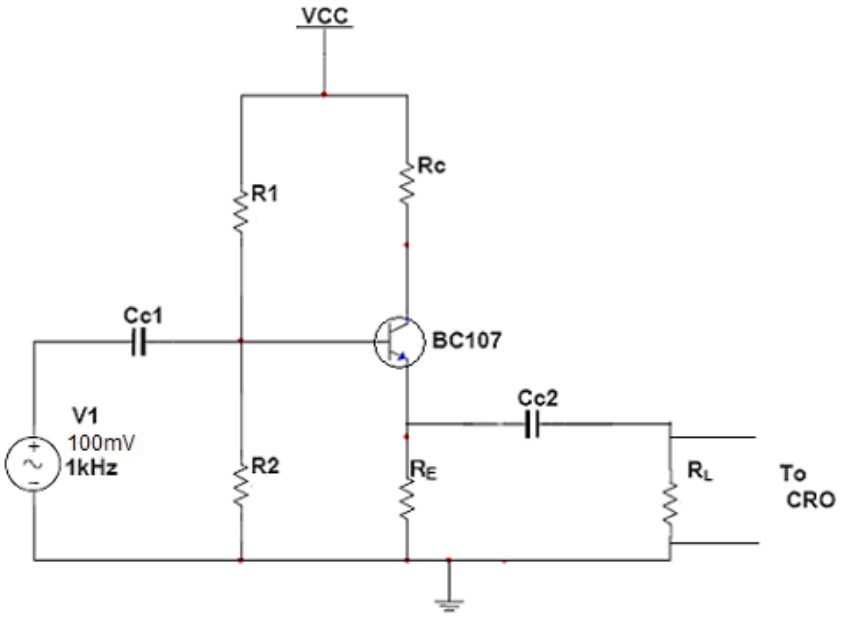
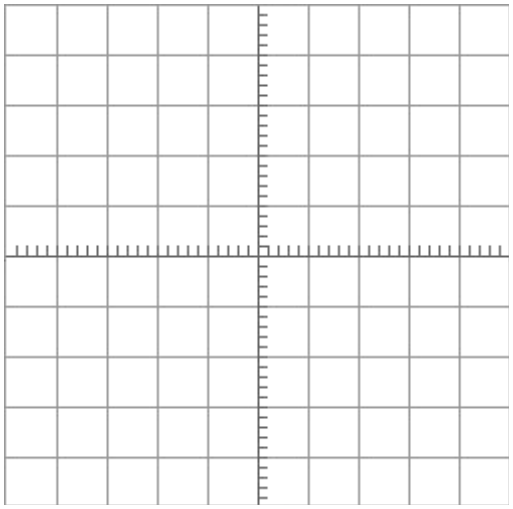


Figure 1

PRACTICE PROCEDURE

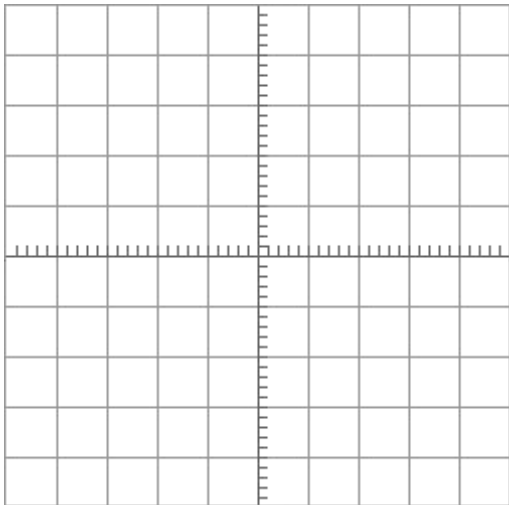
1. Connect the circuit as shown in Figure 1.
2. Apply the bias voltage Vcc and check the dc bias voltages at test points.
3. Apply an input sine wave signal of 100mV, 1 kHz from the function generator.
4. Observe the output in CRO. Calculate the corresponding gain and compare with the designed values.
5. Vary the frequency of the input signal and tabulate the output signal gain for different frequencies.
6. Plot the Frequency Vs Gain (dB) using semilog sheet and calculate the bandwidth of the given amplifier from the plot.

Volt/div = Time/div =



Graph 1: Input sine wave

Volt/div = Time/div =



Graph 2: Output Waveform

Inference

Table1: Frequency response with bypass capacitor

Input voltage, Vs = mV

Input frequency (Hz)	Output voltage, Vo (volts)	Gain = Vo / Vs	20 log Gain (Gain in dB)
10			
20			
50			
100			
200			
500			
1k			
2k			
5k			
10k			
20k			
50k			
100k			
200k			
500k			
1M			

Instructor_____

Inference

UNDERSTANDING & LEARNING

RESULTS AND CONCLUSION

Prepared by:
Name: _____ Reg. No.: _____

Experiment Date: ……

Report Submission Date: ……

Submission Delay: ….....

Signature

ASSESSMENT

Student Task	Max. Marks	Graded Marks
Pre-lab Preparation	15	
Performance	10	
Observation & Inference	10	
Post-lab / Viva-voce	15	
Total	50	