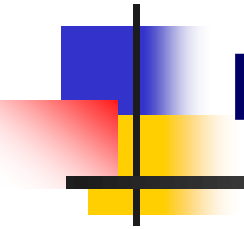


FPGA Based System Design

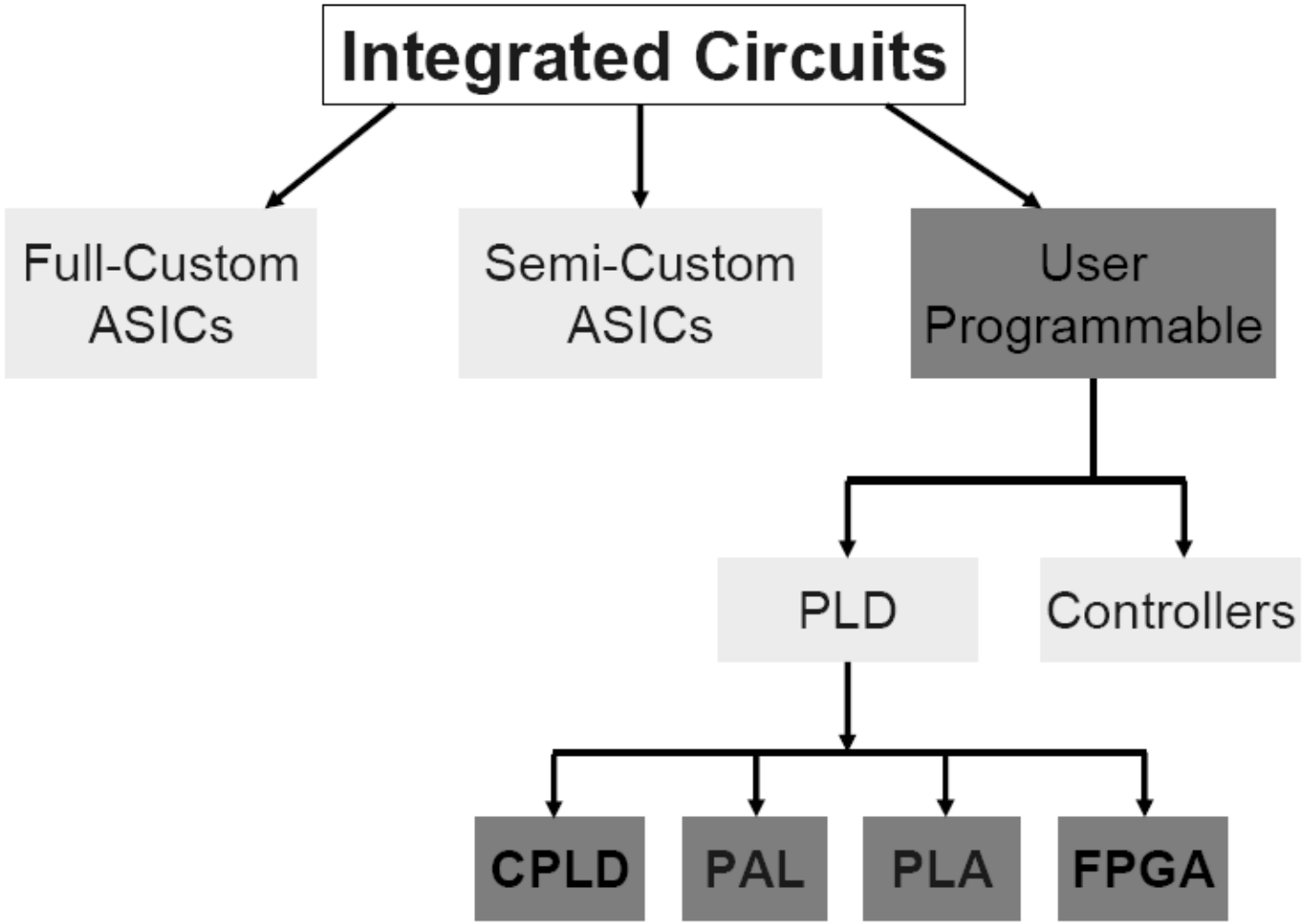
Reference

- Wayne Wolf, ‘FPGA-Based System Design’ Pearson Education, 2004

Why VLSI?

- Integration improves the design:
  - higher speed;
  - lower power;
  - physically smaller.
- Integration reduces manufacturing cost (almost) - no manual assembly.

Integrated Circuits



Full Custom ICs

- Can achieve very high transistor density (transistors per square micron)
- design time can be very long (multiple months).
- Involves the creation of a completely new chip, which consists of masks (for the photolithographic manufacturing process)
- Benefits - Excellent performance, small size, low power

Standard Cell

- Designer uses a library of standard cells
- an automatic place and route tool does the layout
- *Transistor density* and performance degradation depends on type of design being done.
- Design time can be much faster than full custom because layout is automatically generated.

Gate Array

- Designer uses a library of standard cells.
- The design is mapped onto an array of transistors which is already created on a wafer
- wafers with transistor arrays can be created ahead of time
- A *routing tool* creates the masks for the routing layers and "customizes" the pre-created gate array for the user's design
- Transistor density can be almost as good as standard cell.
- Design time advantages are the same as for standard cell.

Semi-custom ICs

- Flexible as portion of the IC is customized by the user
- Suitable for specific applications
- Gate array + standard cell
- Paves way for application specific ICs (ASIC)

Role of FPGA

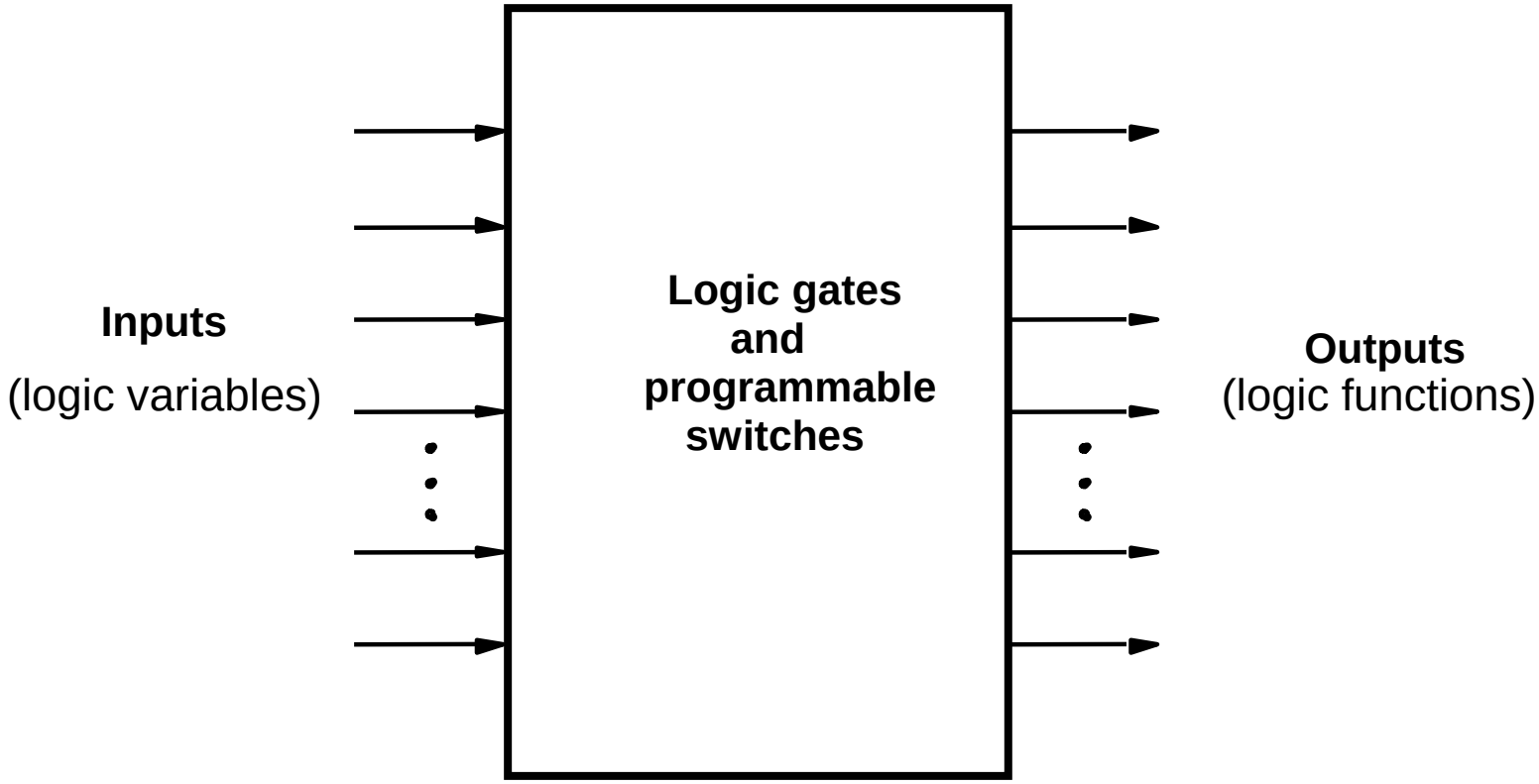
- Microprocessors used in variety of environments
  - Rely on software to implement functions
  - Generally slower and more power-hungry than custom chips
- When FPGAs?
  - Design economics
    - Shortest time to market
    - Lowest NRE cost
    - Highest unit cost
  - Make quick grab for market share
  - Same FPGA reused in several designs

Programmable logic devices

- Programmable Logic Device (PLD):
  - An integrated circuit chip that can be configured by end user to implement different digital hardware
  - Also known as “Field Programmable Logic Device (FPLD) “

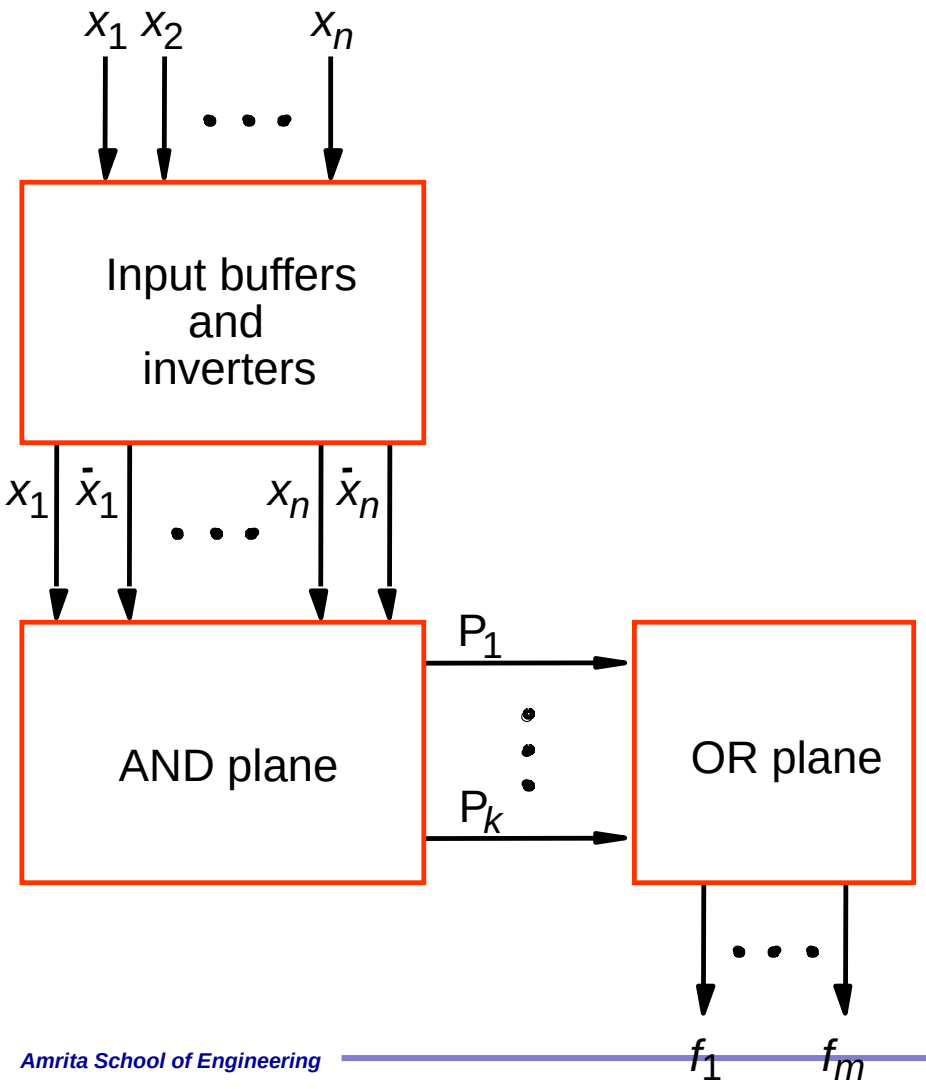
PLD

- PLD as a Black Box



Programmable Logic Array (PLA)

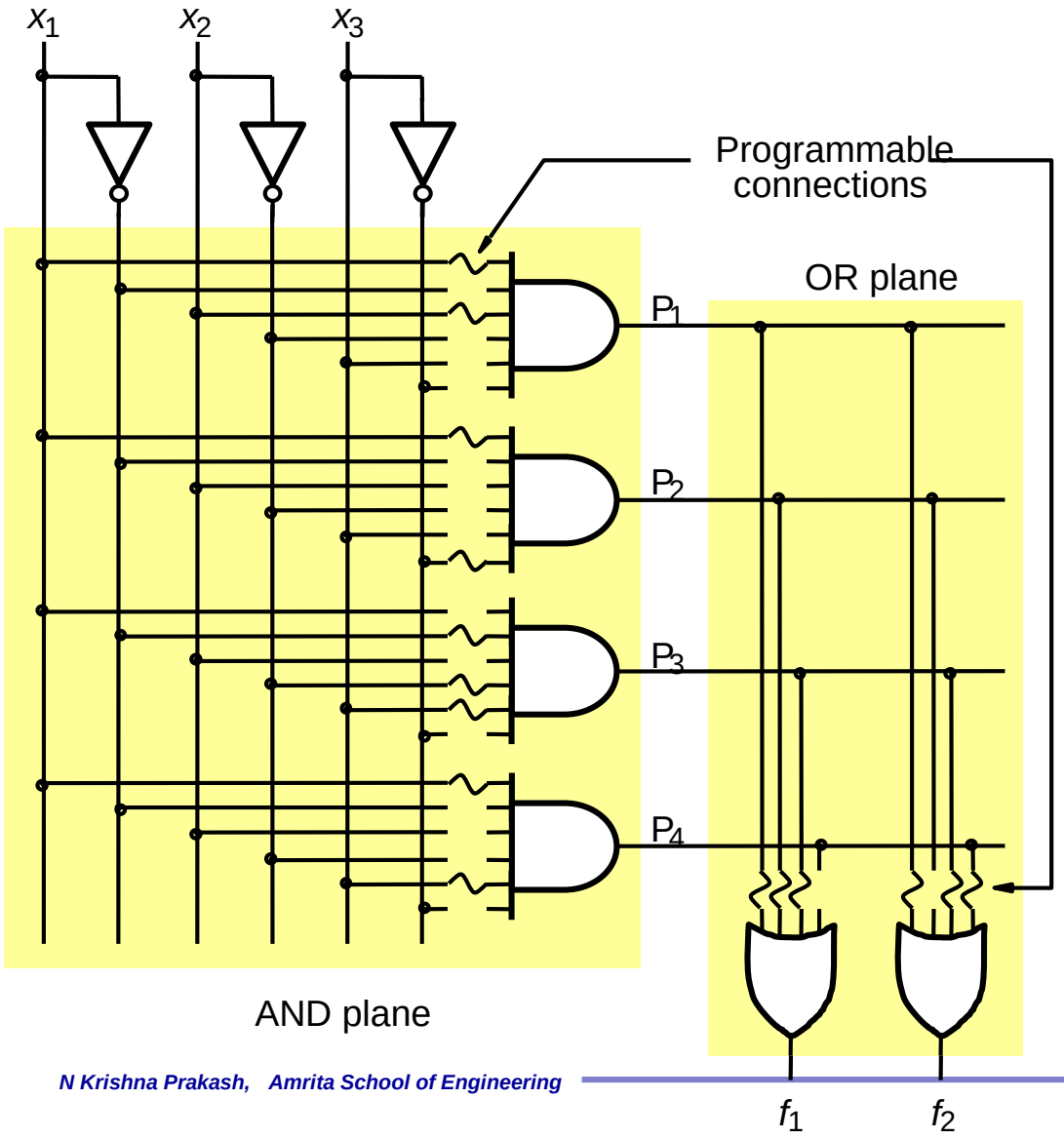
- Use to implement circuits in SOP form
- The connections in the AND plane are programmable
- The connections in the OR plane are programmable



Gate Level Version of PLA

$f_1 = x_1x_2+x_1x_3'+x_1'x_2'x_3$

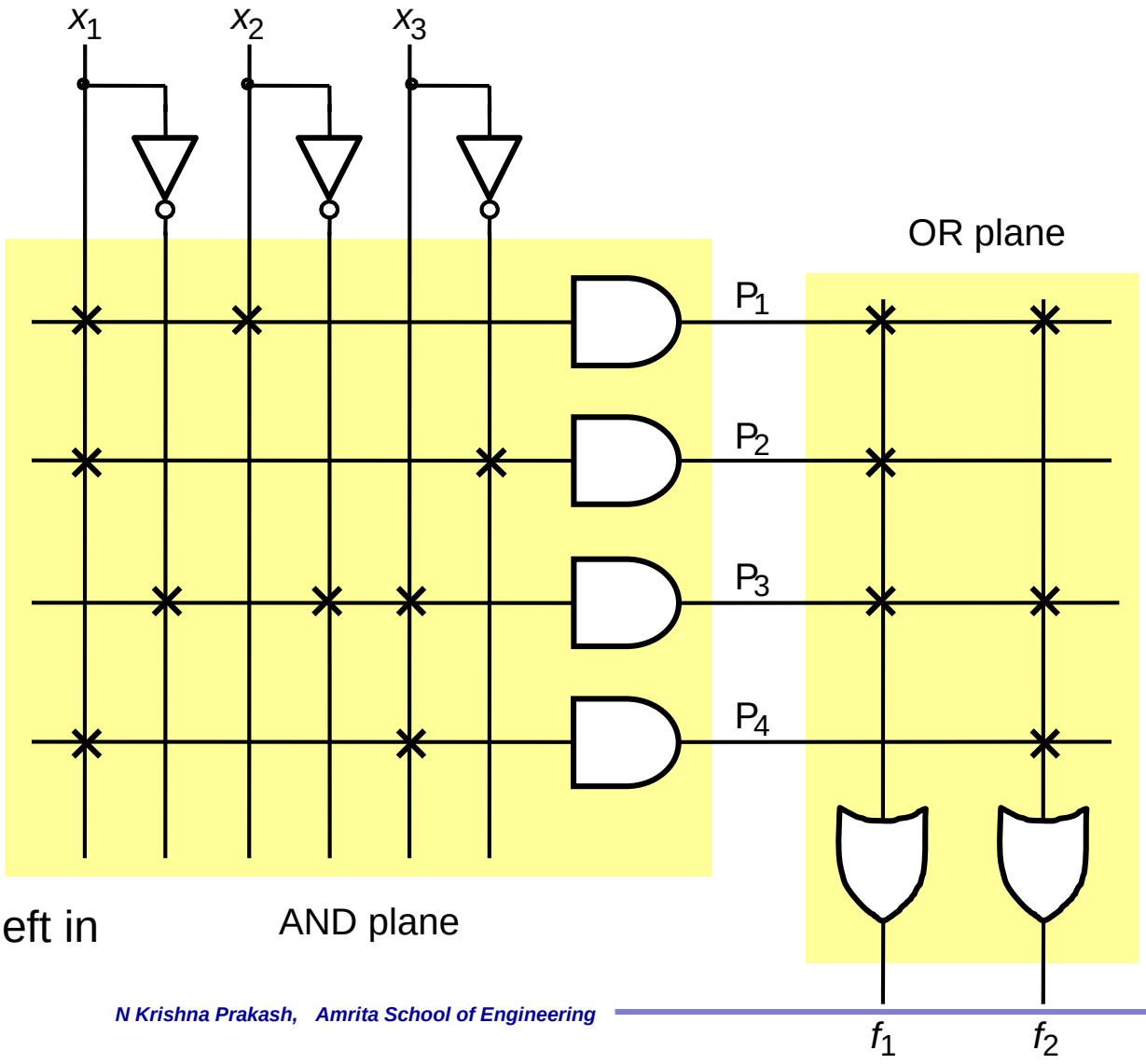
$f_2 = x_1x_2+x_1'x_2'x_3+x_1x_3$



Customary Schematic of a PLA

$f_1 = x_1x_2+x_1x_3'+x_1'x_2'x_3$

$f_2 = x_1x_2+x_1'x_2'x_3+x_1x_3$



x marks the connections left in place after programming

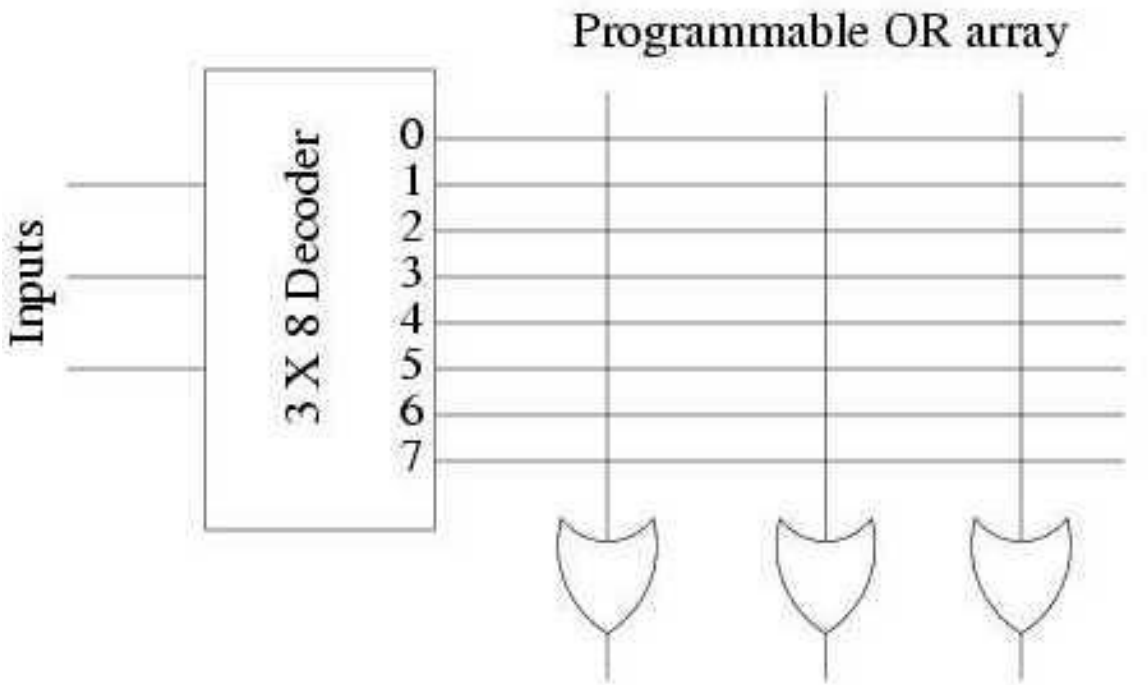
Limitations of PLAs

- Typical size is 16 inputs, 32 product terms, 8 outputs
  - Each AND gate has large fan-in - this limits the number of inputs that can be provided in a PLA
  - 16 inputs → 2^{16} = possible input combinations; only 32 permitted (since 32 AND gates) in a typical PLA
  - 32 AND terms permitted → large fan-in for OR gates as well
- This makes PLAs slower and slightly more expensive than some alternatives to be discussed shortly

Programmable ROM (PROM)

- Address: N bits; Output word: M bits
- ROM contains 2 N words of M bits each
- The input bits decide the particular word that becomes available on output lines

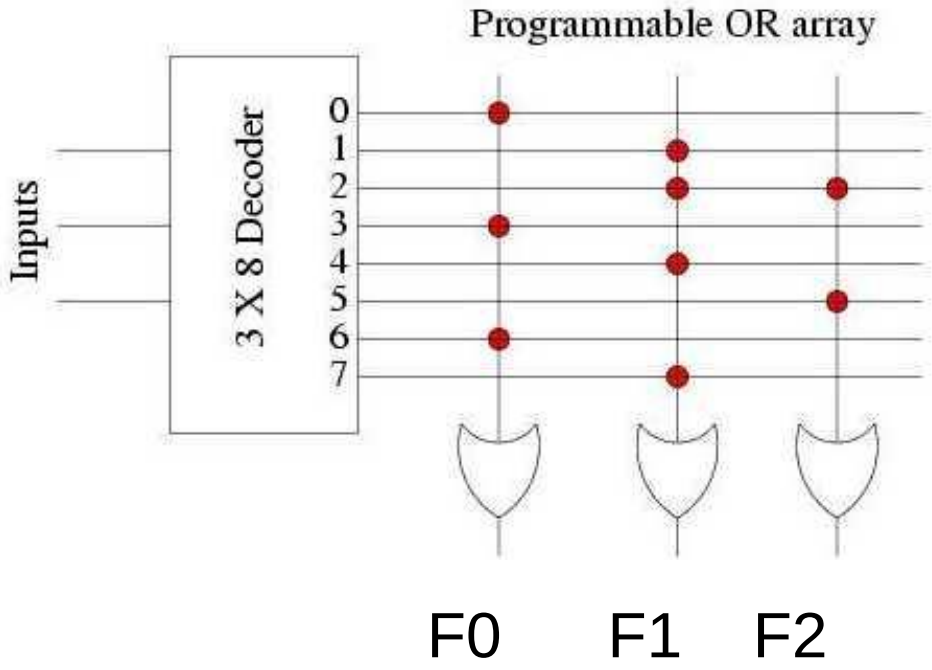
Logic Diagram of 8x3 PROM



Sum of minterms

Combinational Circuit Implementation using PROM

I0	I1	I2	F0	F1	F2
0	0	0	1	0	0
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	1	0
1	0	1	0	0	1
1	1	0	1	0	0
1	1	1	0	1	0



PROM Types

- Programmable PROM
  - Break links through current pulses
  - Write once, Read multiple times
- Erasable PROM (EPROM)
  - Program with ultraviolet light
  - Write multiple times, Read multiple times
- Electrically Erasable PROM (EEPROM)/ Flash Memory
  - Program with electrical signal
  - Write multiple times, Read multiple times

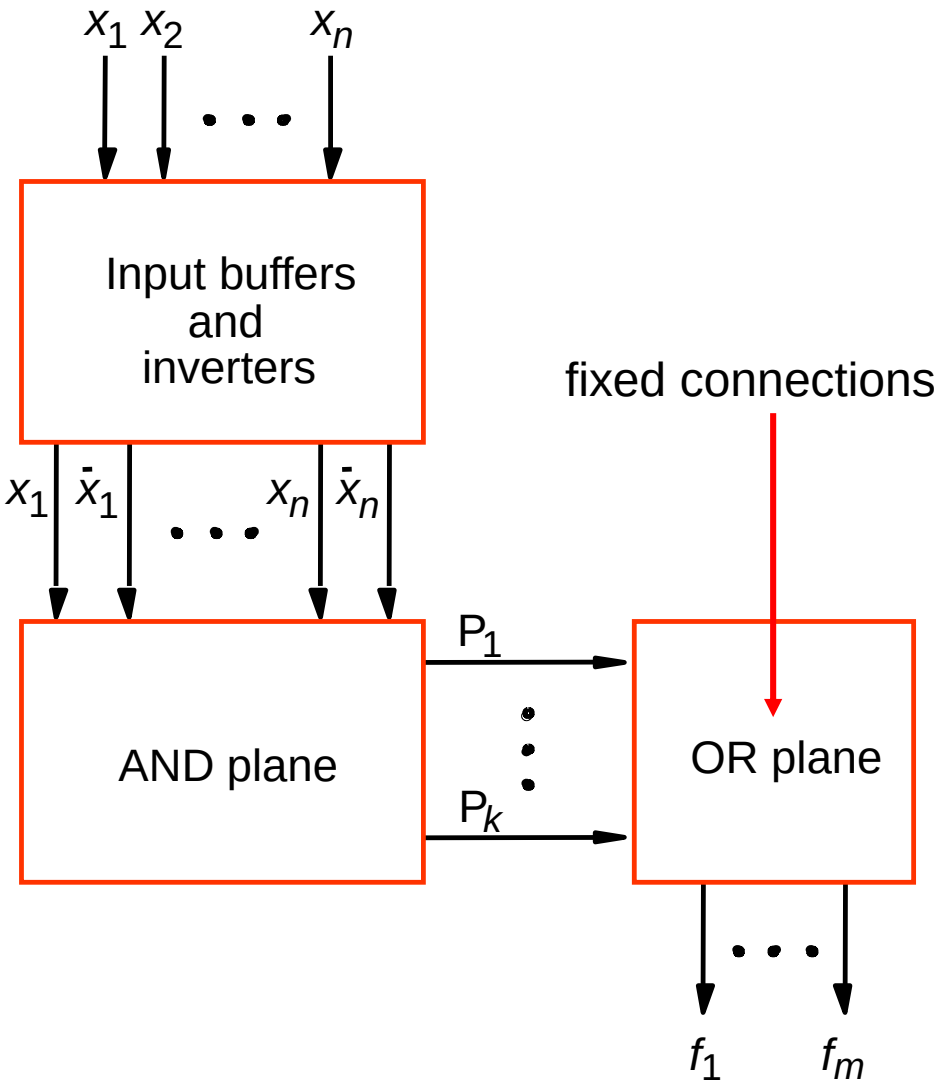
PROM: Advantages and Disadvantages

- Widely used to implement functions with large number of inputs and outputs

- For combinational circuits with lots of don't care terms, PROM is a wastage of logic resources

Programmable Array Logic (PAL)

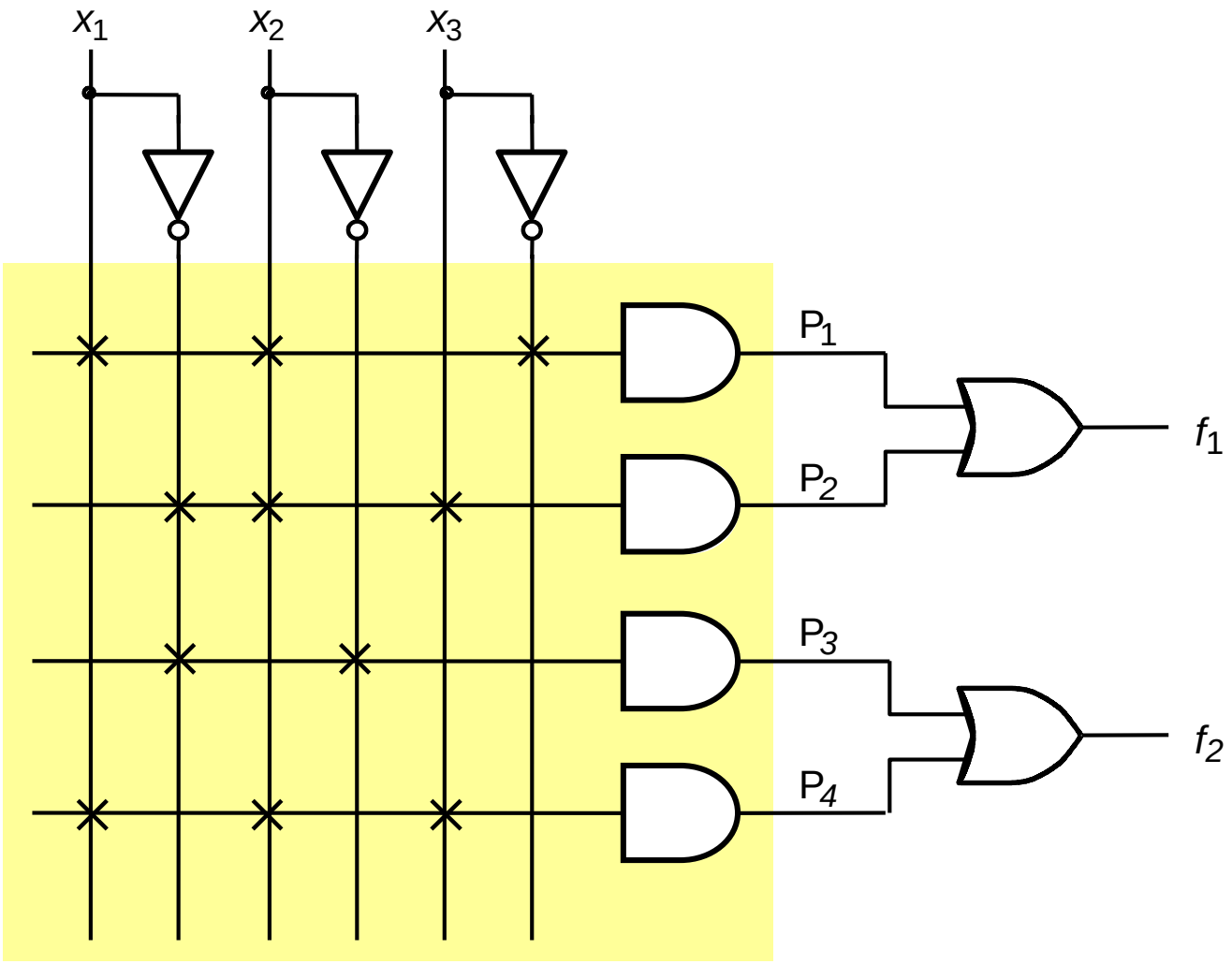
- Also used to implement circuits in SOP form
- The connections in the AND plane are programmable
- The connections in the OR plane are NOT programmable

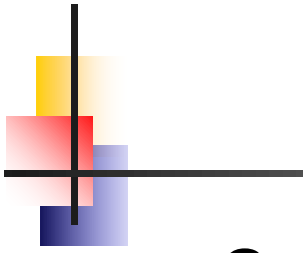


Example Schematic of a PAL

$f_1 = x_1x_2x_3'+x_1'x_2x_3$

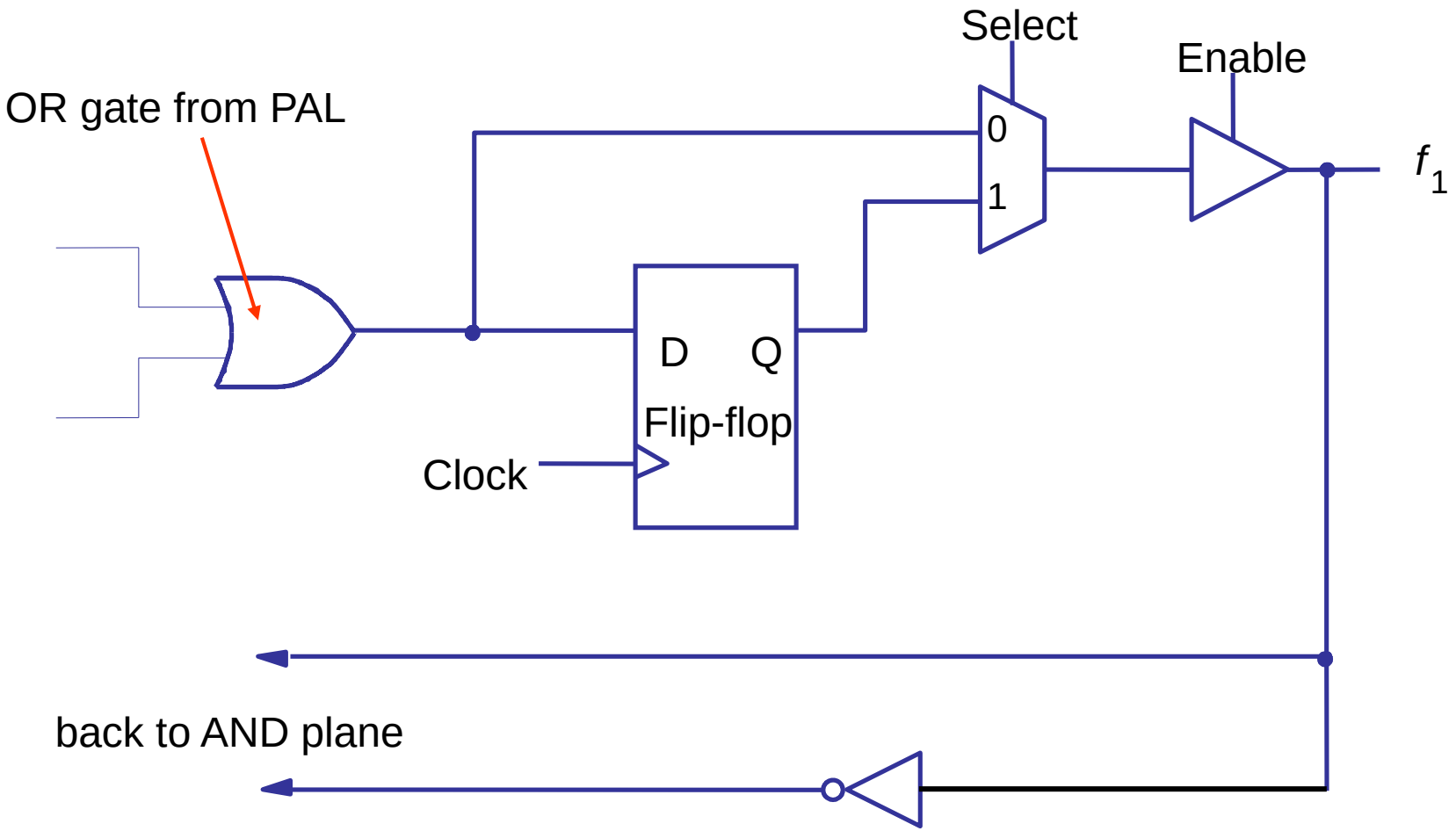
$f_2 = x_1'x_2'+x_1x_2x_3$





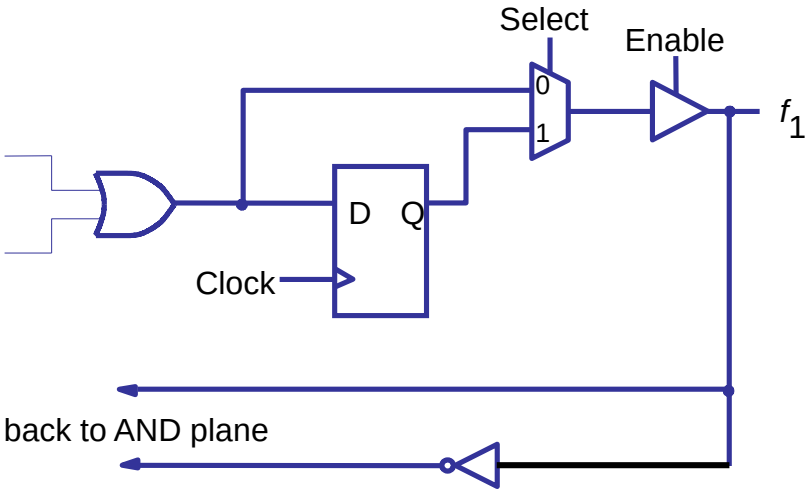
- Comparing PALs and PLAs
  - PALs have the same limitations as PLAs (small number of allowed AND terms) plus they have a fixed OR plane → less flexibility than PLAs
  - PALs are simpler to manufacture, cheaper, and faster (better performance)
  - PALs also often have extra circuitry connected to the output of each OR gate
    - The OR gate plus this circuitry is called a *macrocell*

Macrocell


Select
Enable
OR gate from PAL
0
1
f_1
D
Q
Flip-flop
Clock
back to AND plane

Macrocell Functions

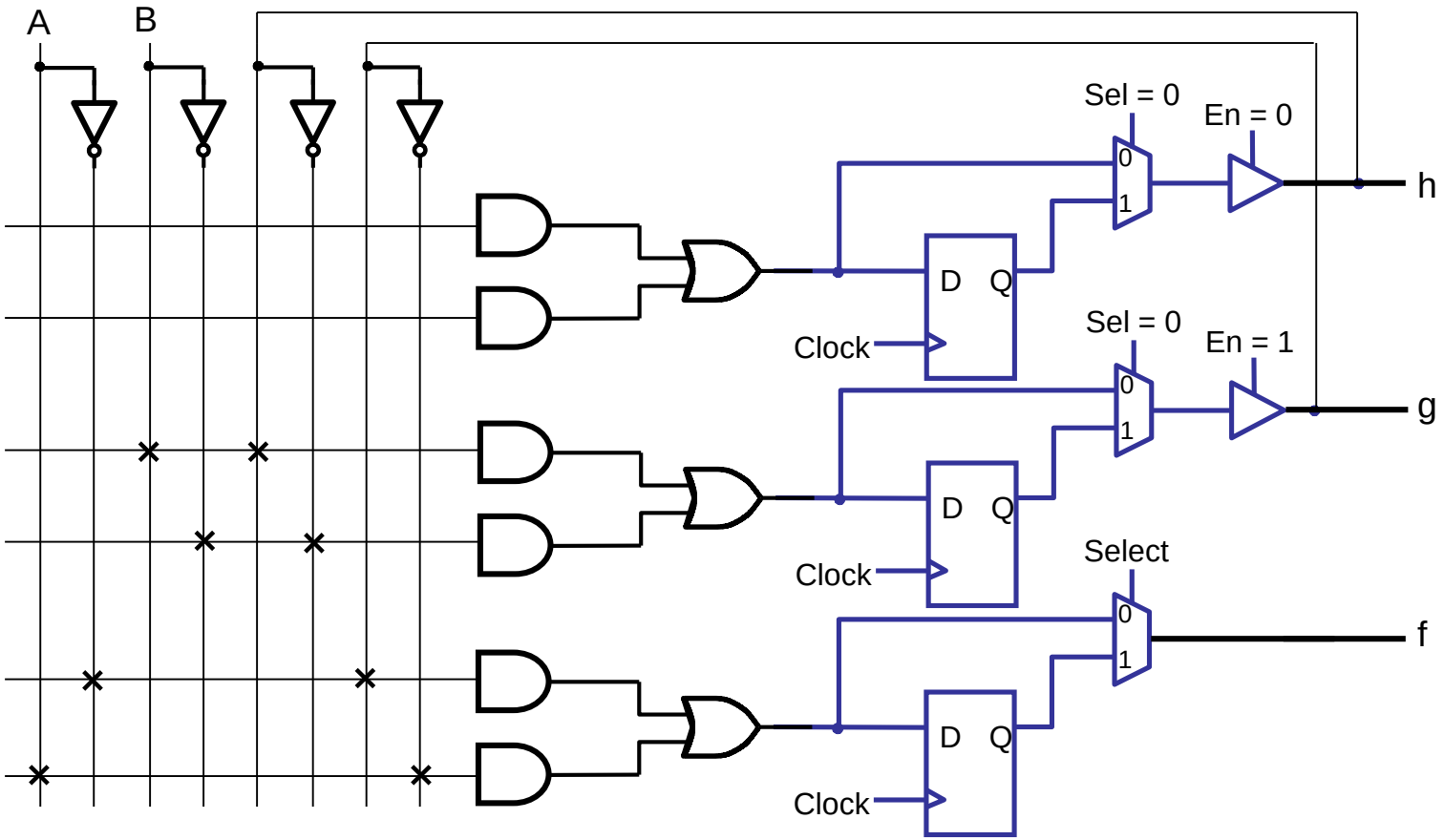
- Enable = 0 can be used to allow the output pin for f_1 to be used as an additional input pin to the PAL
- Enable = 1, Select = 0 is normal for typical PAL operation
- Enable = Select = 1 allows the PAL to synchronize the output changes with a clock pulse



- The feedback to the AND plane provides for multi-level design

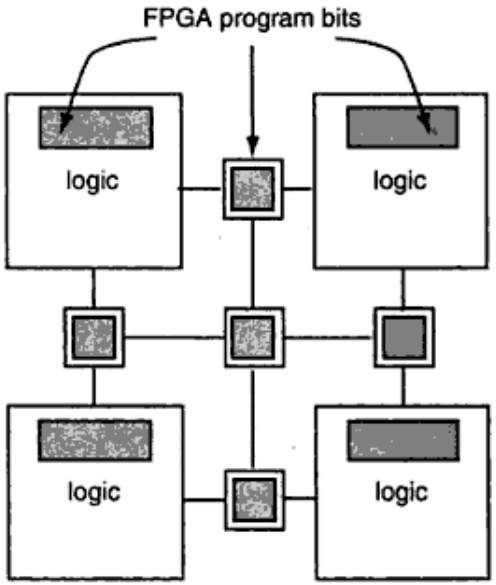
Multi-Level Design with PALs

- f = A'BC + A'B'C' + ABC' + AB'C = A'g + Ag'
  - where g = BC + B'C' and C = h below



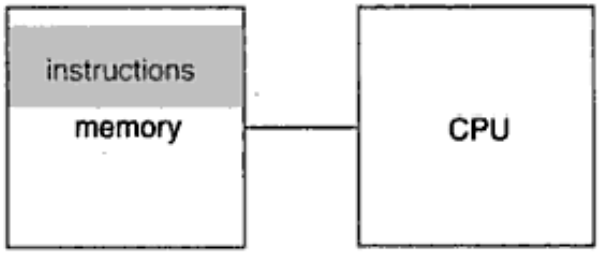
FPGA Programming

- FPGAs implement multi-level logic
- Need both programmable logic blocks and programmable interconnect
- Combination of logic and interconnect is fabric



FPGA

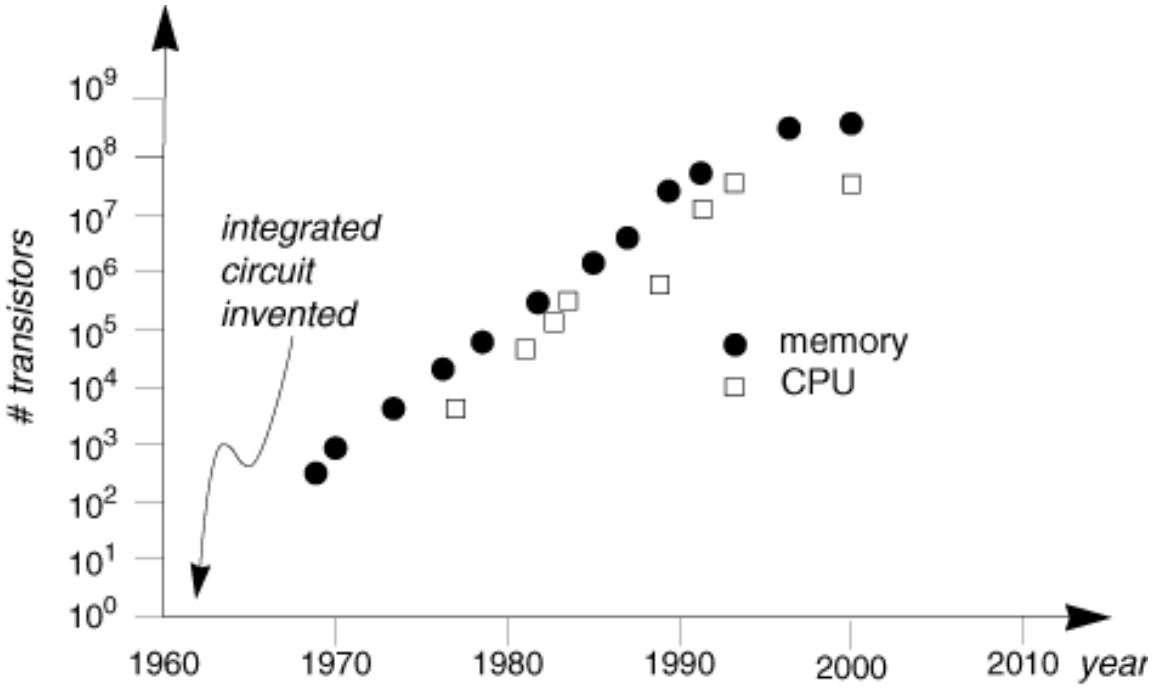
- Microprocessor is a stored-program computer



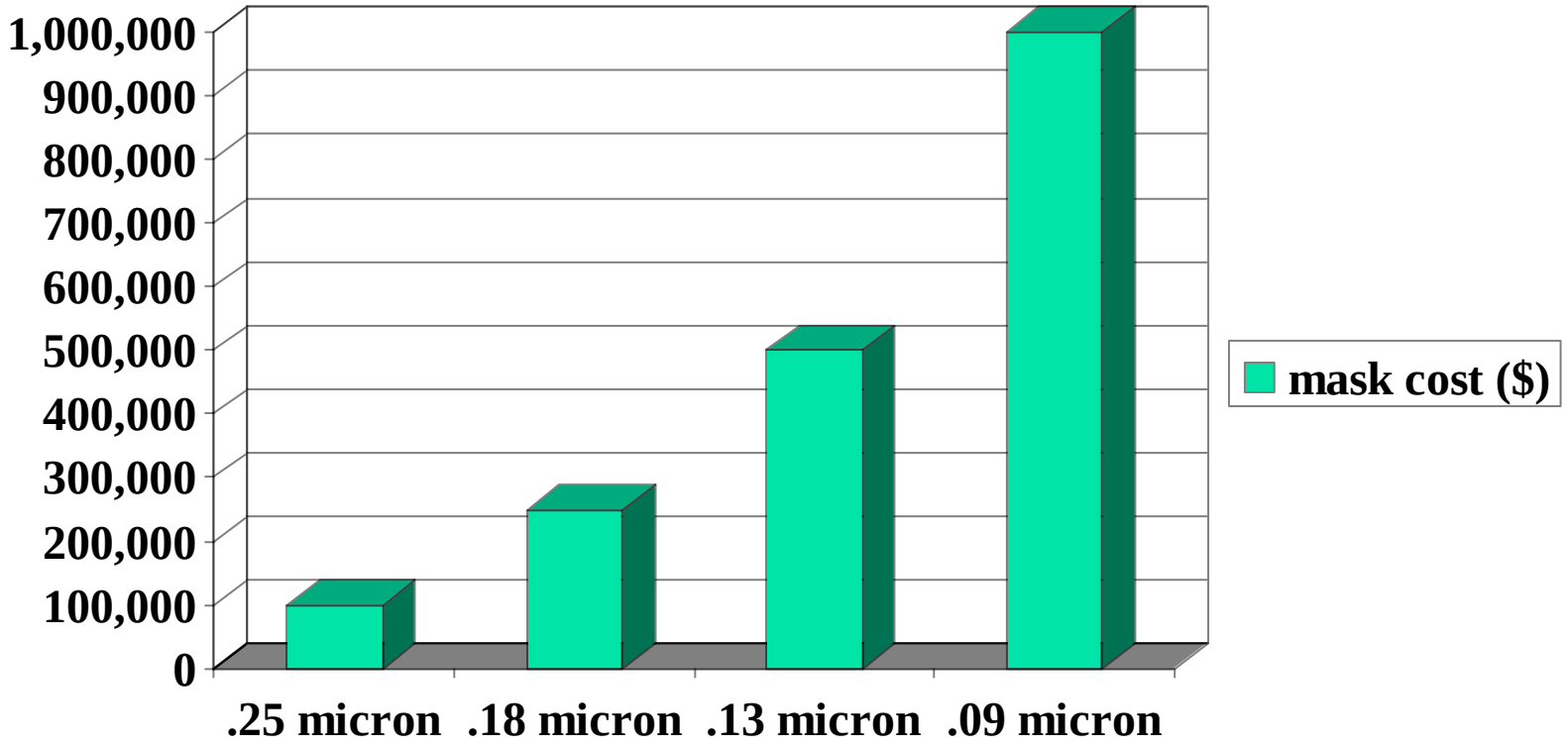
microprocessor

Moore's Law

- Gordon Moore: co-founder of Intel.
- Predicted that number of transistors per chip would grow exponentially (double every 18 months).



Mask cost Vs technology line width



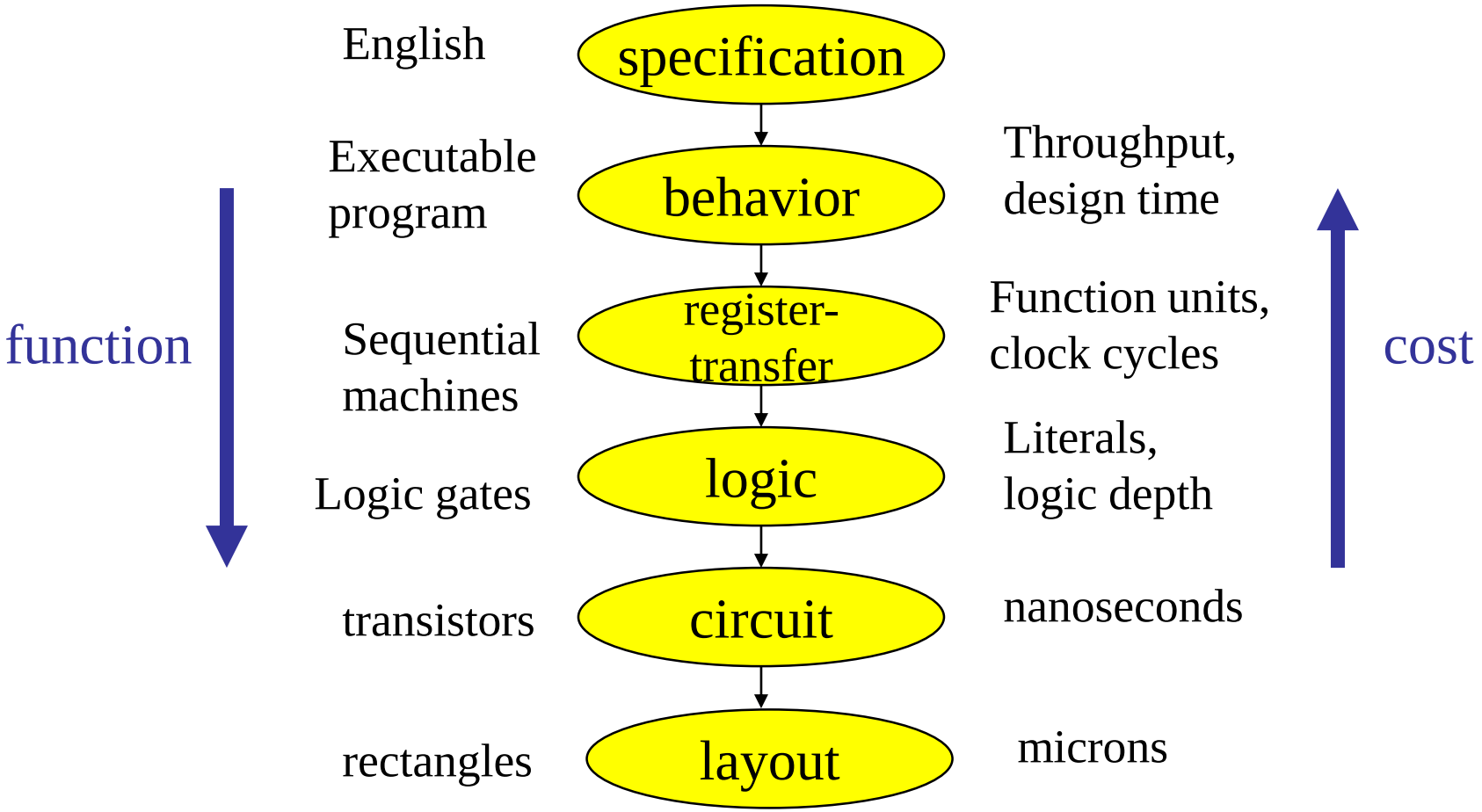
Goals and Techniques

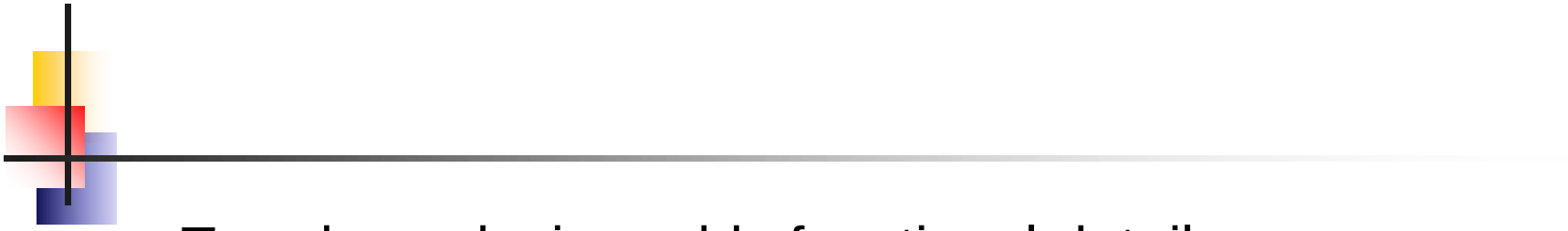
- Performance
  - Logic rate
- Power/energy
- Design time
- Design cost
  - FPGA tools less expensive than custom VLSI tools
- Manufacturing cost

Design Challenges

- Multiple levels of abstraction
- Power consumption
- Short design time

FPGA Abstractions





- Top-down design adds functional detail.
  - Create lower levels of abstraction from upper levels.
- Bottom-up design creates abstractions from low-level behavior.
- Good design needs both top-down and bottom-up efforts.

Methodology

- Hardware Description logic (HDL)
  - VHDL
  - VerilogHDL

Major FPGA Vendors

- SRAM-based FPGAs
  - **Xilinx, Inc**
  - **Altera Corp.**
  - Atmel
  - Lattice Semiconductor

Share 80% of the market

- Flash & Antifuse FPGAs
  - Actel Corp.
  - Quick logic Corp.

FPGA Vendors and Device families

- Xilinx
  - Spartan
  - Virtex
  - Kintex
  - Artix
- Altera
  - Stratix
  - Cyclone
  - MAX 3000/7000 CPLD
  - MAX-II

Xilinx Families

- **Old families**
  - XC3000, XC4000, XC5200
  - Old 0.5µm, 0.35µm and 0.25µm technology. Not recommended for modern designs.
- **High-performance families**
  - Virtex (0.22µm)
  - Virtex-E, Virtex-EM (0.18µm)
  - Virtex-II, Virtex-II PRO (0.13µm)
  - Virtex-4 (0.09µm)
- **Low Cost Family**
  - Spartan/XL – derived from XC4000
  - Spartan-II – derived from Virtex
  - Spartan-IIE – derived from Virtex-E
  - Spartan-3 – derived from Virtex-II

Altera Families

- **Old Families**
  - FLEX 10K, FLEX 6000, FLEX 8000
- **High-performance Families**
  - Mercury
  - Stratix, Stratix GX, Stratix II
  - APEX 20K , APEX II
  - Excalibur
- **Low Cost Family**
  - Cyclone, Cyclone II