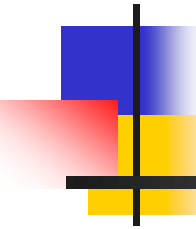


FPGA Fabrics

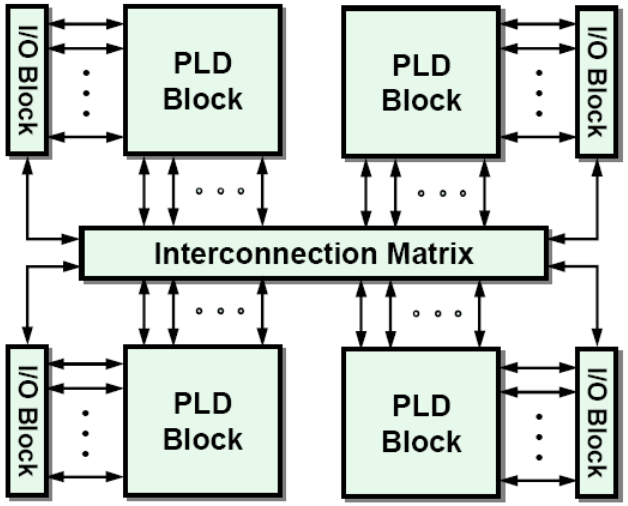
Reference

- Wayne Wolf, ‘FPGA-Based System Design’ Pearson Education, 2004

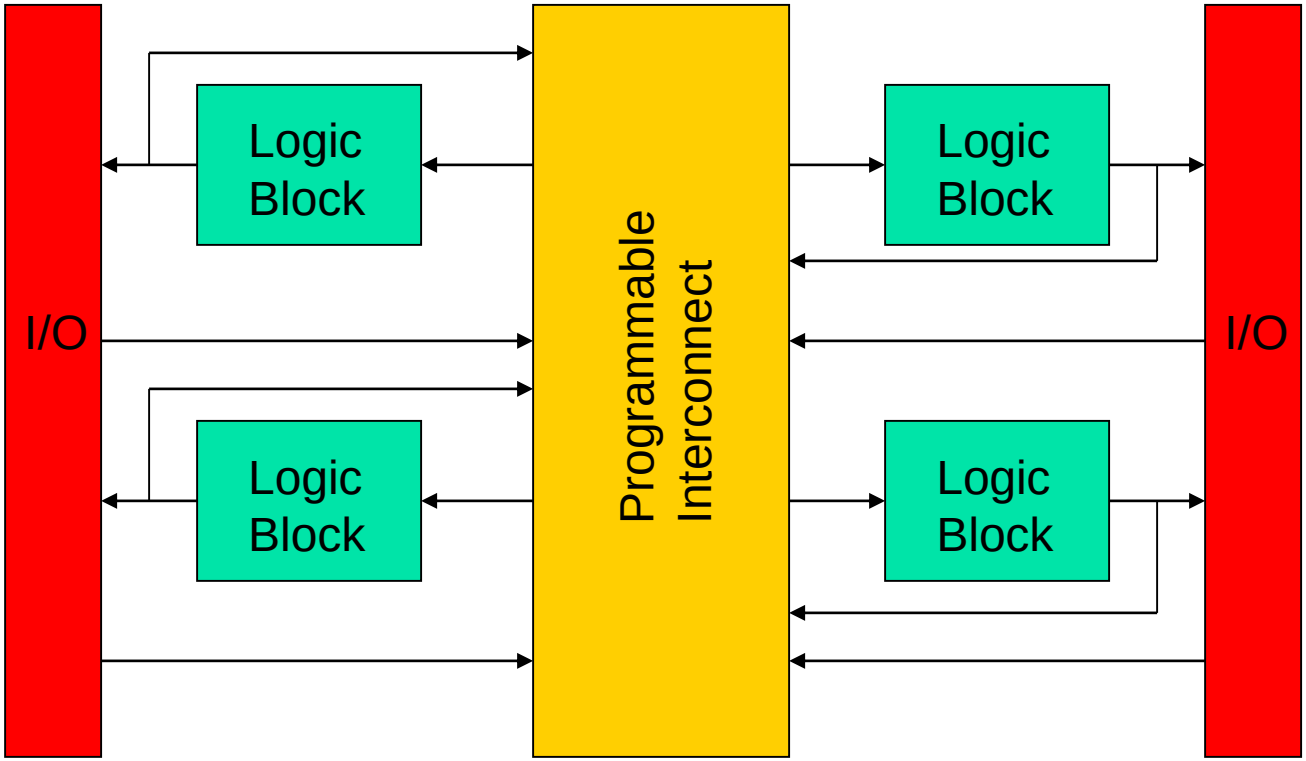
CPLD / FPGA

CPLD

- Interconnection of several PLD blocks with Programmable interconnect on a single chip
- Logic blocks executes sum-of-product expressions and stores the results in micro-cell registers
- Programmable interconnects route signals to and from logic blocks



CPLD

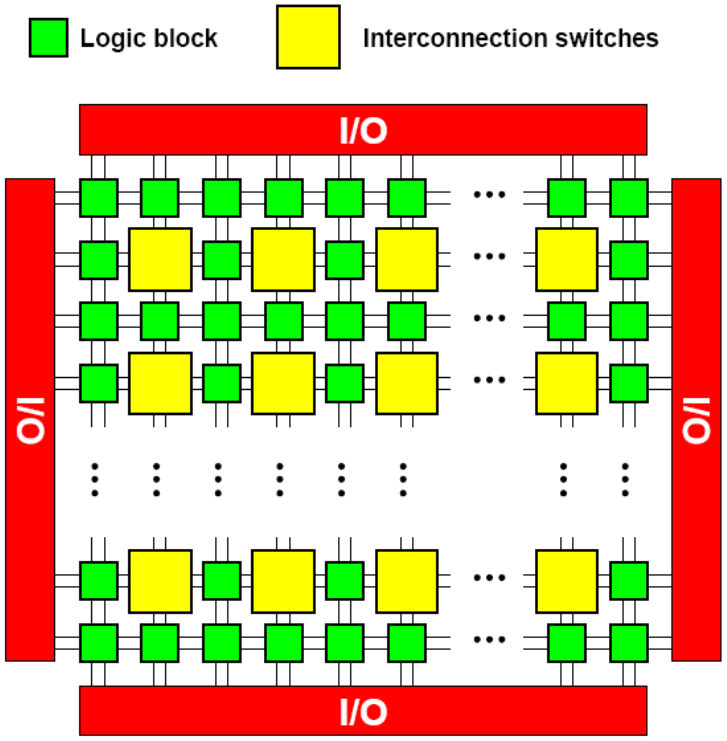

I/O
Logic Block
Logic Block
Programmable Interconnect
Logic Block
Logic Block
I/O

Major CPLD Resources

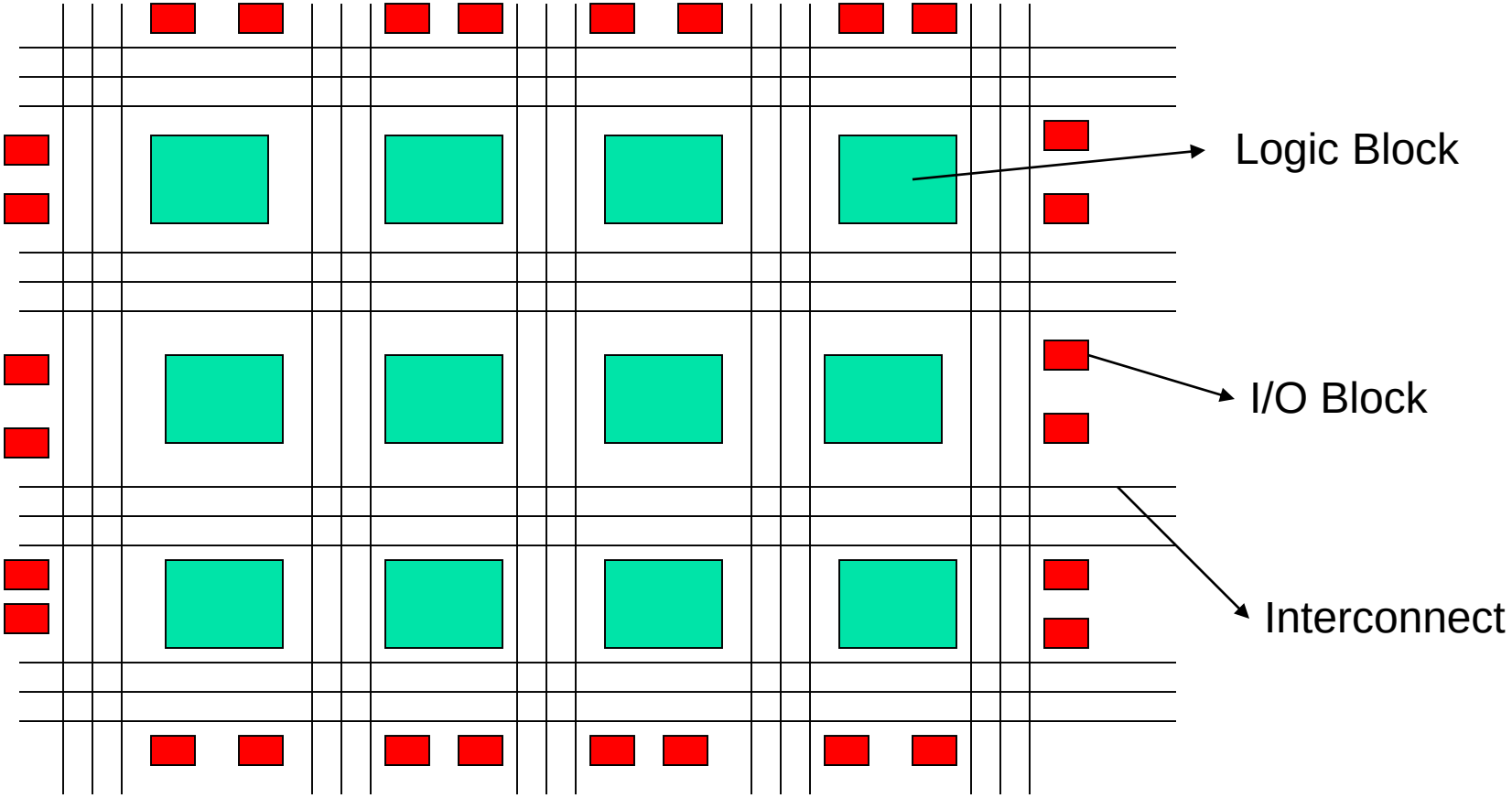
- Number of macro-cells per logic block
- Number of inputs from programmable interconnect to logic block
- Number of product terms in logic block

FPGA

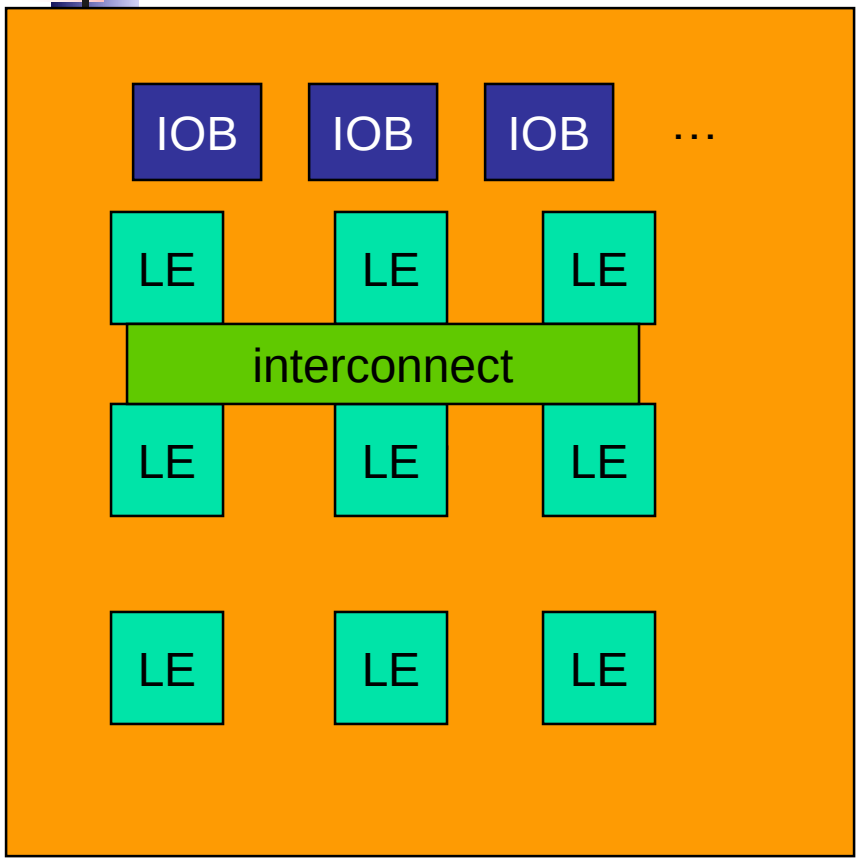
- Programmable Logic Blocks
  - Implement combinational & sequential logic
- Programmable Interconnect
  - Wires to connect inputs and outputs to logic blocks
- Programmable I/O blocks
  - Logic blocks at the periphery for external connections



Structure of FPGA



FPGA Fabric



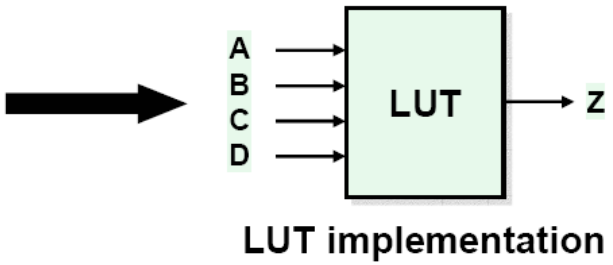
- CLB: combinational logic block = logic element (LE).
- LUT: Lookup table = SRAM used for truth table.
- I/O block (IOB): I/O pin + associated logic and electronics.

FPGA Fabric

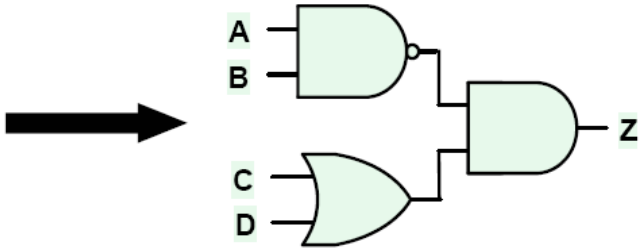
- Look-up table with N-inputs can be used to implement any combinational function of N-inputs
- LUT is programmed with truth table

A	B	C	D	Z
0	0	0	0	**0**
0	0	0	1	**1**
0	0	1	0	**1**
0	0	1	1	**1**
0	1	0	0	**0**
0	1	0	1	**1**
0	1	1	0	**1**
0	1	1	1	**1**
1	0	0	0	**0**
1	0	0	1	**1**
1	0	1	0	**1**
1	0	1	1	**1**
1	1	0	0	**0**
1	1	0	1	**0**
1	1	1	0	**0**

Truth-table

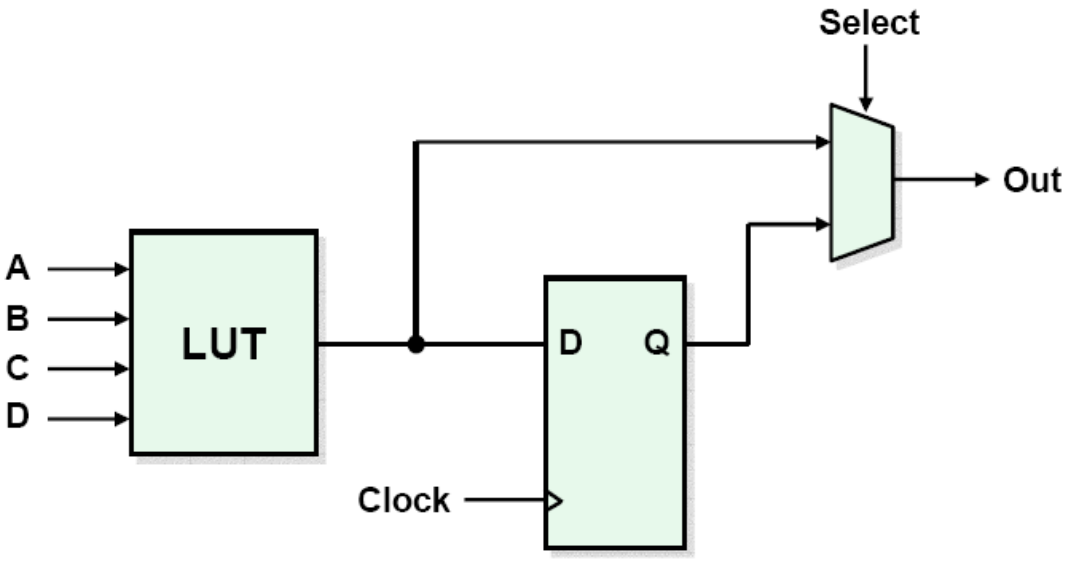


LUT implementation



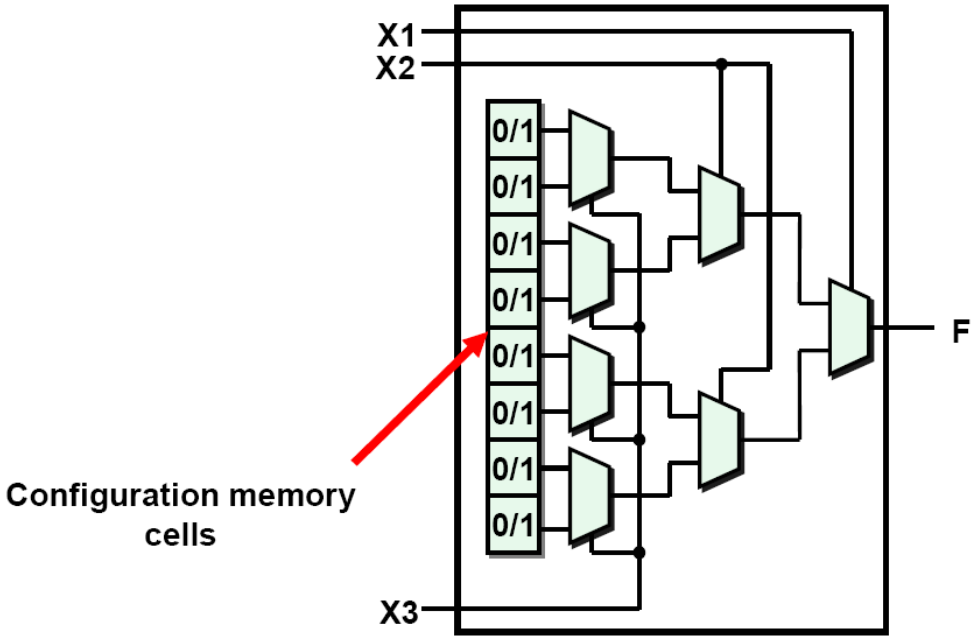
Gate implementation

FPGA Fabric

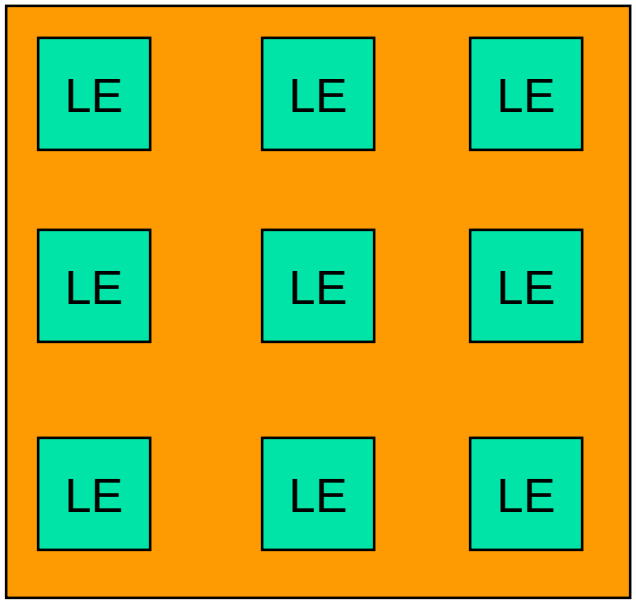


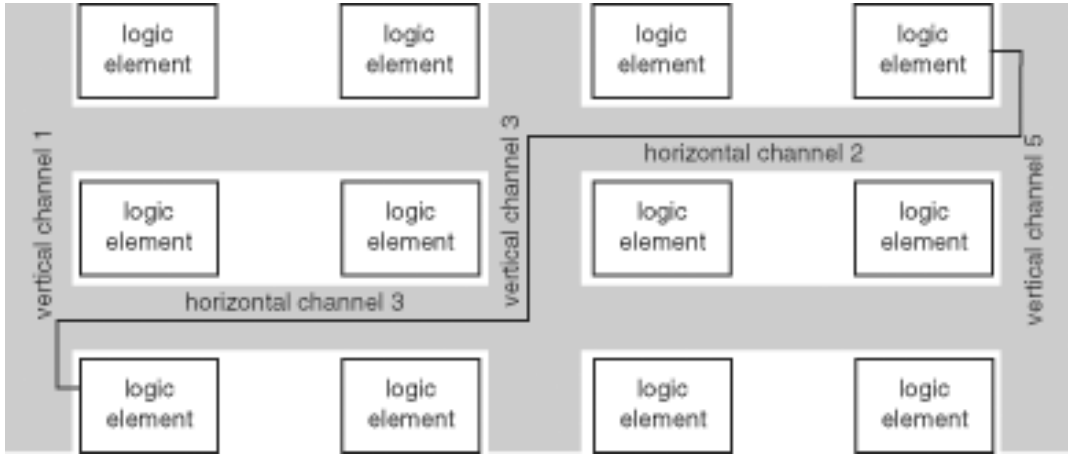
LUT

- 3-input LUT
- Based on Multiplexers
- LUT entries stored in configuration memory cells

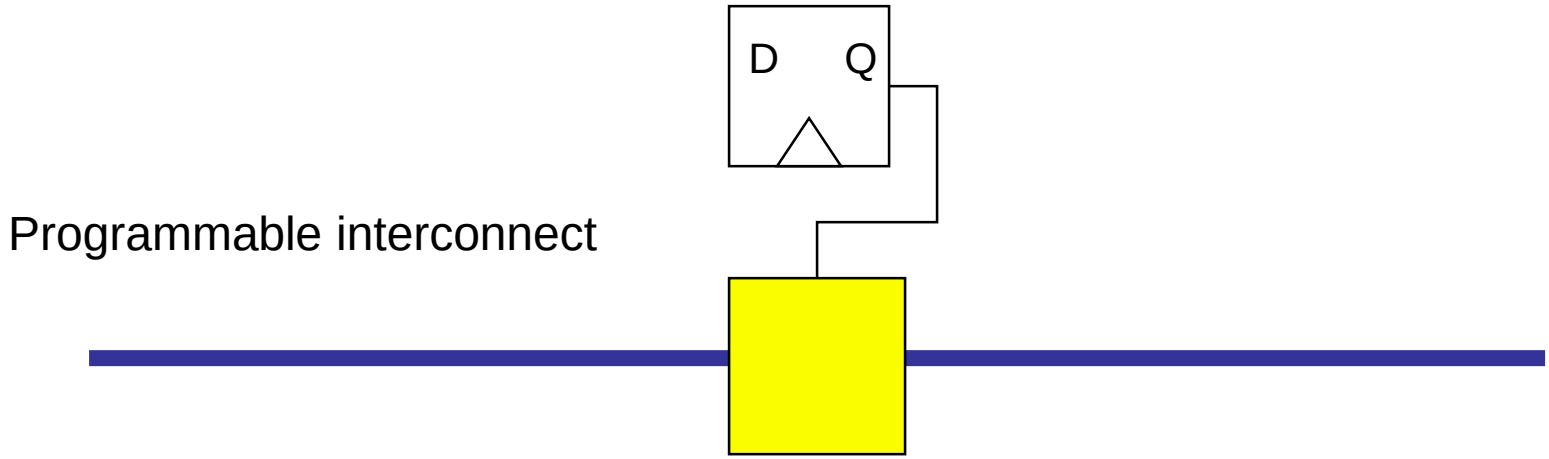


FPGA Fabric (contd)

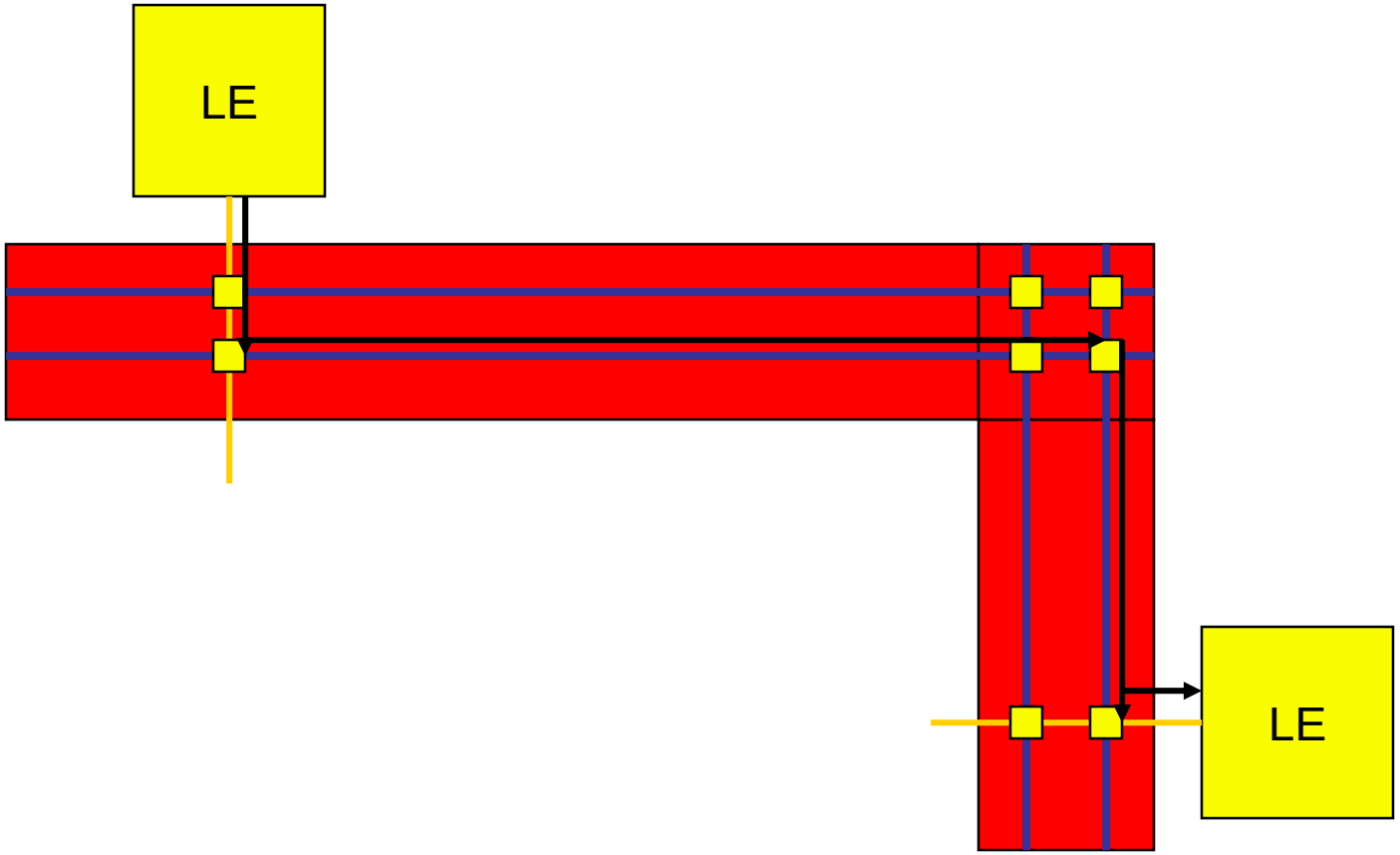




- Organized into channels.
  - Many wires per channel.
- Connections between wires made at programmable interconnection points.
- Must choose:
  - Channels from source to destination.
  - Wires within the channels.



Choosing a Path

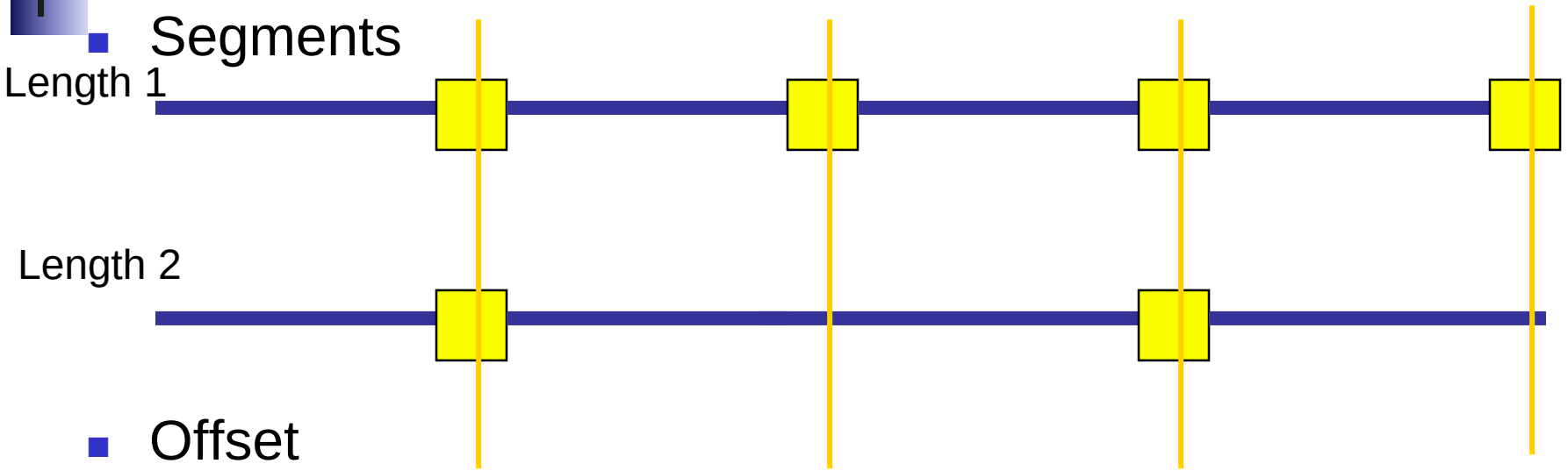


Routing Problems

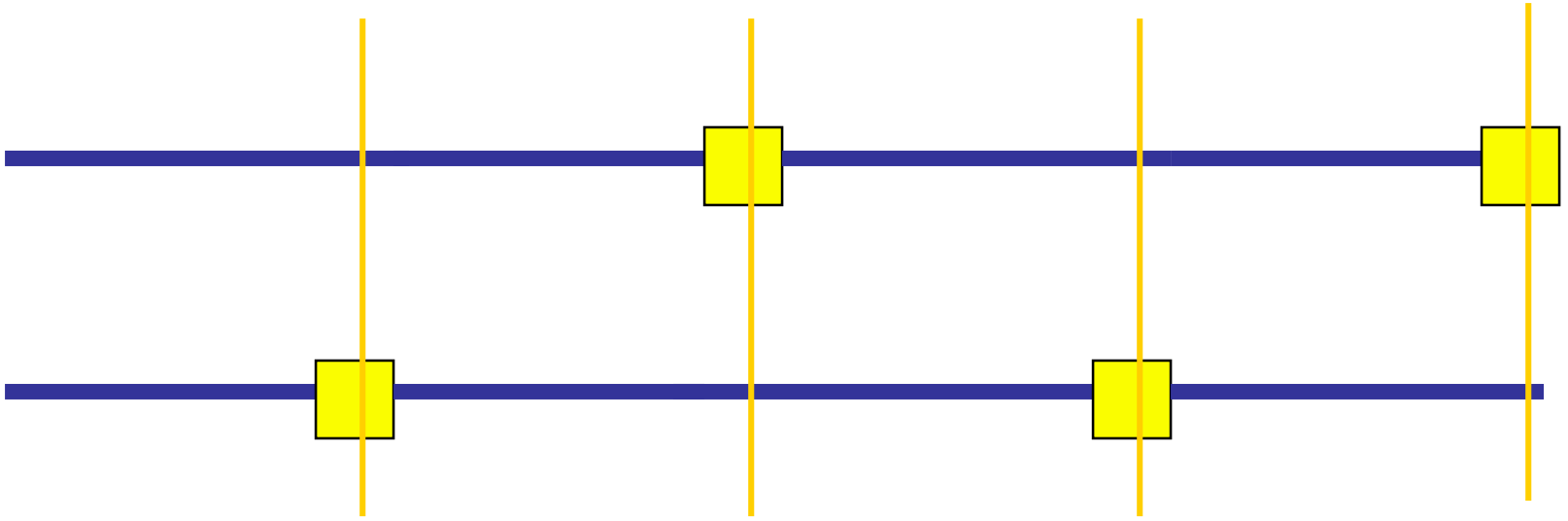
- Global routing:
  - Which combination of channels?
- Local routing:
  - Which wire in each channel?
- Routing metrics:
  - Net length.
  - Delay.

Segmented wiring Vs Offset wiring

- Segments



- Offset



SRAM-based FPGA fabrics

- Xilinx
- Altera

SRAM-based FPGAs

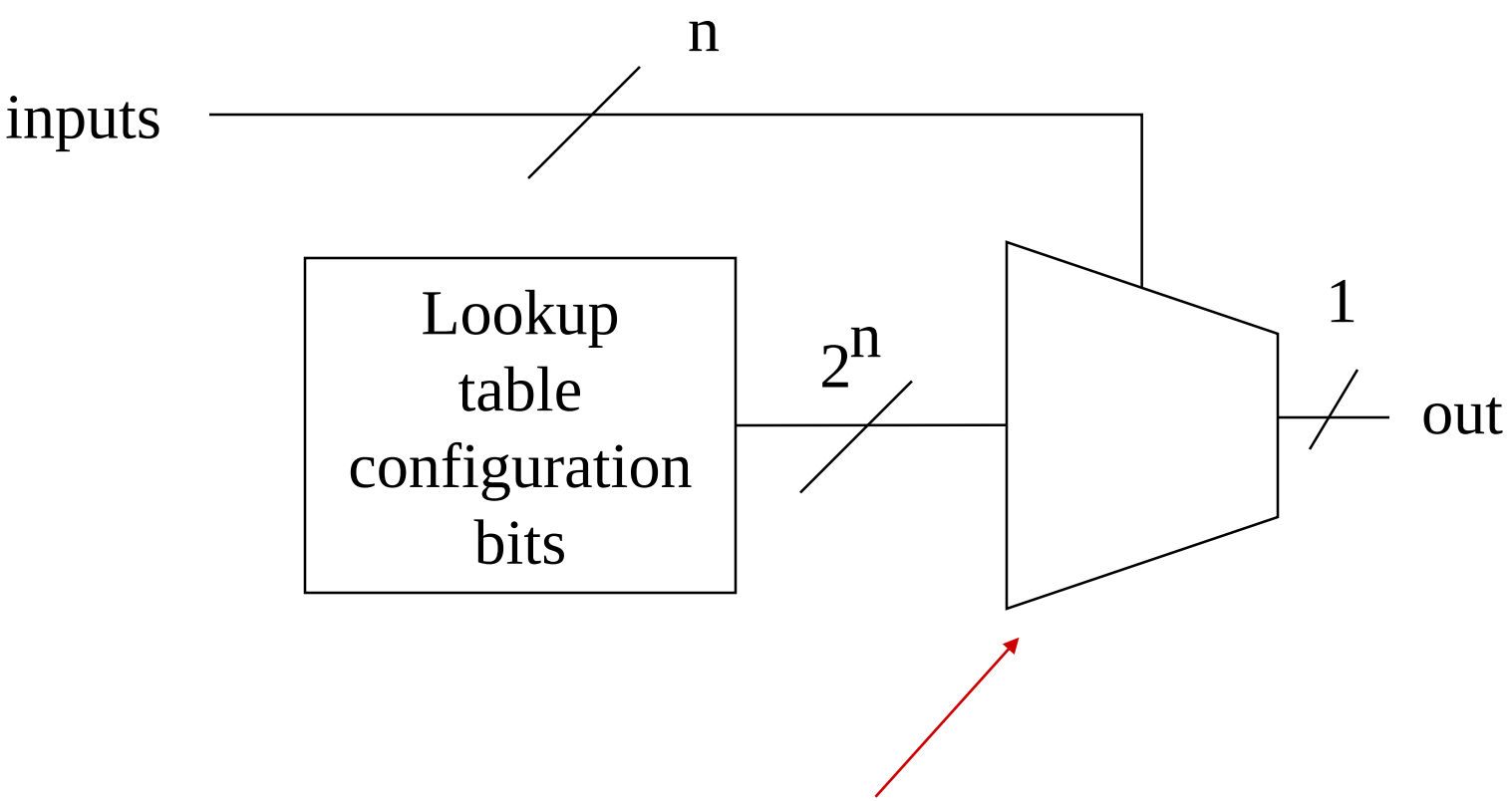
- Program logic functions, interconnect using SRAM.
- Advantages:
  - Re-programmable;
  - dynamically reconfigurable;
  - Fabricated with standard VLSI processes.
- Disadvantages:
  - SRAM burns power.
  - Possible to steal, disrupt configuration bits.

Logic elements

- Logic element includes combinational function + register(s).

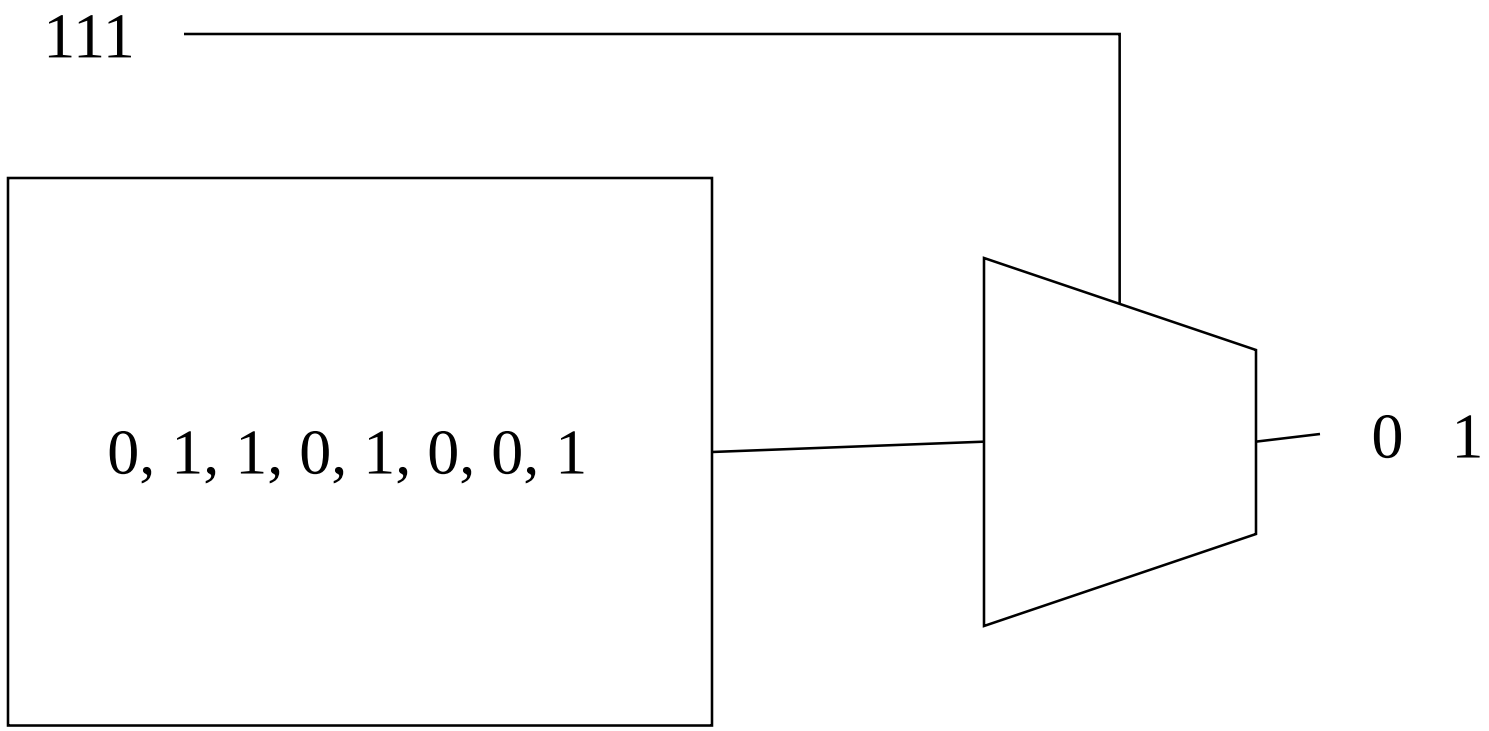
- Use SRAM as lookup table LUT for combinational function.

LUT-based logic element



Can multiplex at output or address at input

Example

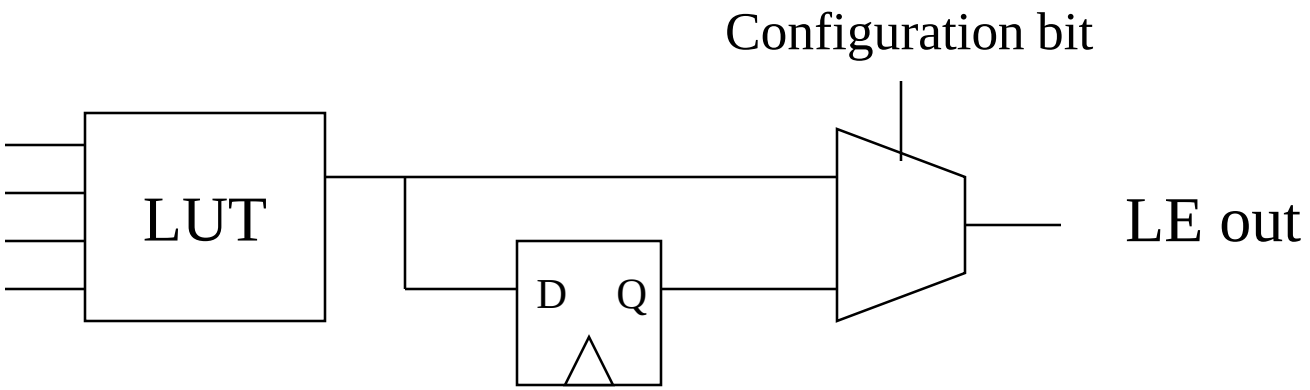


Evaluation of SRAM-based LUT

- N-input LUT can handle function of 2^n inputs.
- All logic functions take the same amount of space.
- All functions have the same delay.
- SRAM is larger than static gate equivalent of function.
- Burns power at idle.
- Want to selectively add register to LE:

Registers in logic elements

- Register may be selected into the circuit:

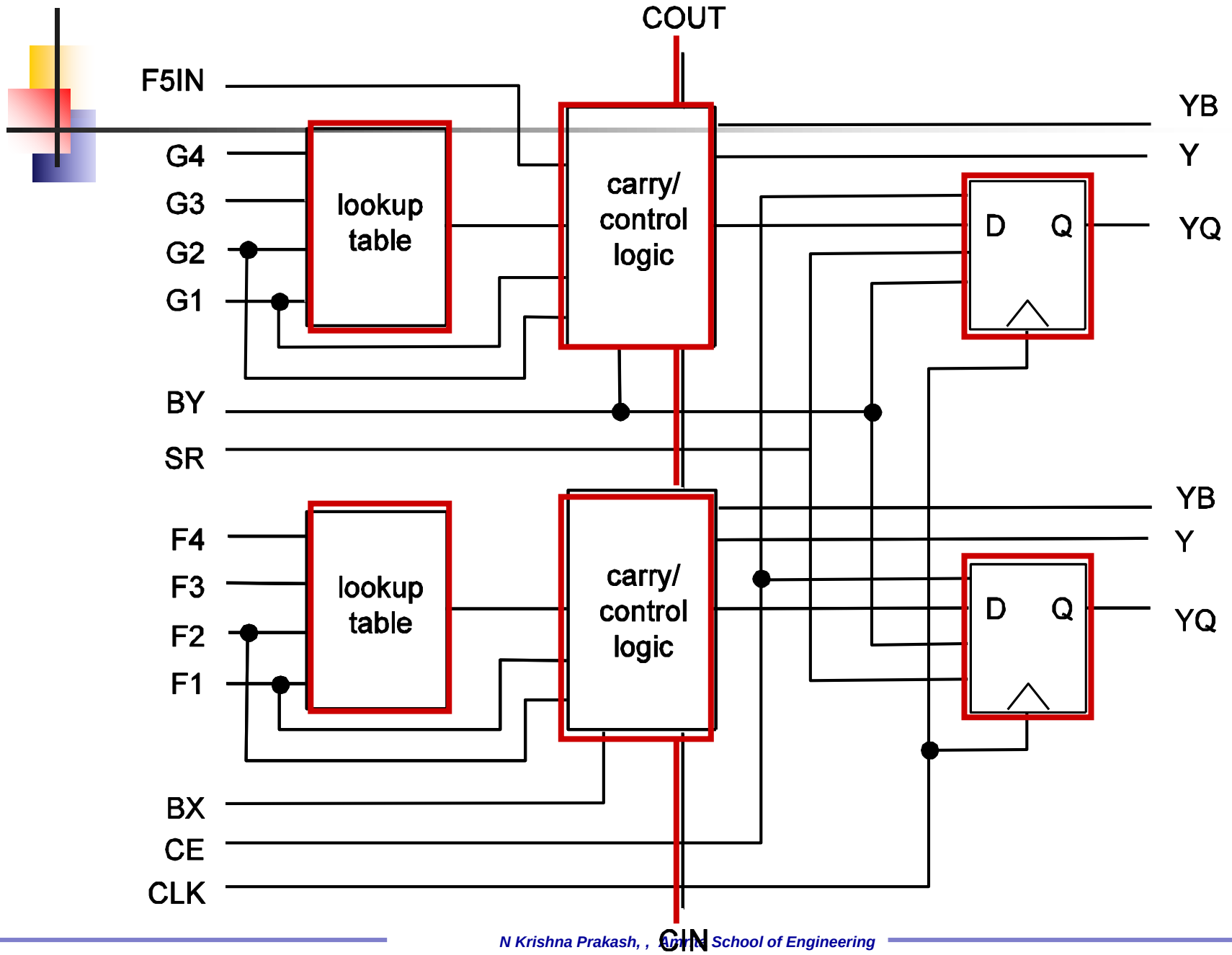


Other LE features

- Multiple logic functions in an LE are possible.
- Specialized Addition logic:
  - carry chain.
- Partitioned lookup tables.

Xilinx Spartan-II CLB

- Each CLB has two identical slices.
- Slice has two logic cells:
  - LUT.
  - Carry/control logic.
  - Registers.


COUT
F5IN
G4
G3
G2
G1
lookup table
carry/ control logic
D
Q
YB
Y
YQ
BY
SR
F4
F3
F2
F1
lookup table
carry/ control logic
D
Q
YB
Y
YQ
BX
CE
CLK
CIN

Spartan-II CLB details

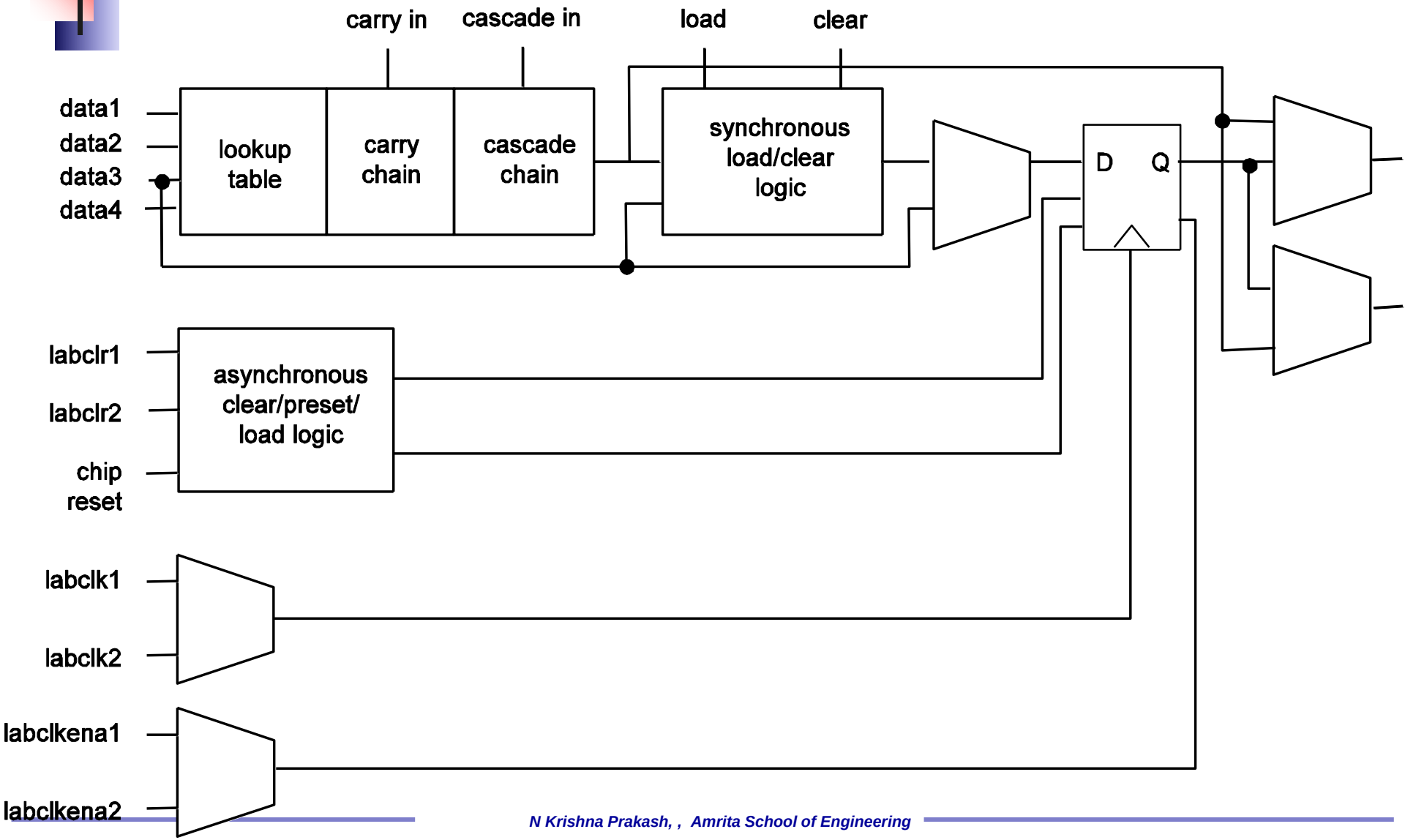
- Each lookup table can be used as a 16-bit synchronous RAM or 16-bit shift register.
- Arithmetic logic includes an XOR gate.
- Each slice includes a mux to combine the results of the two function generators in the slice.
- Register can be configured as DFF or latch.

Spartan-II CLB operation

- Arithmetic:
  - Carry block includes XOR gate.
  - Use LUT for carry, XOR for sum.
- Each slice uses F5 mux to combine results of multiplexers.
- F6 mux combines outputs of F5 muxes.
- Registers can be FF/latch; clock and clock enable.
- Includes three-state output for on-chip bus.

Altera APEX II logic element

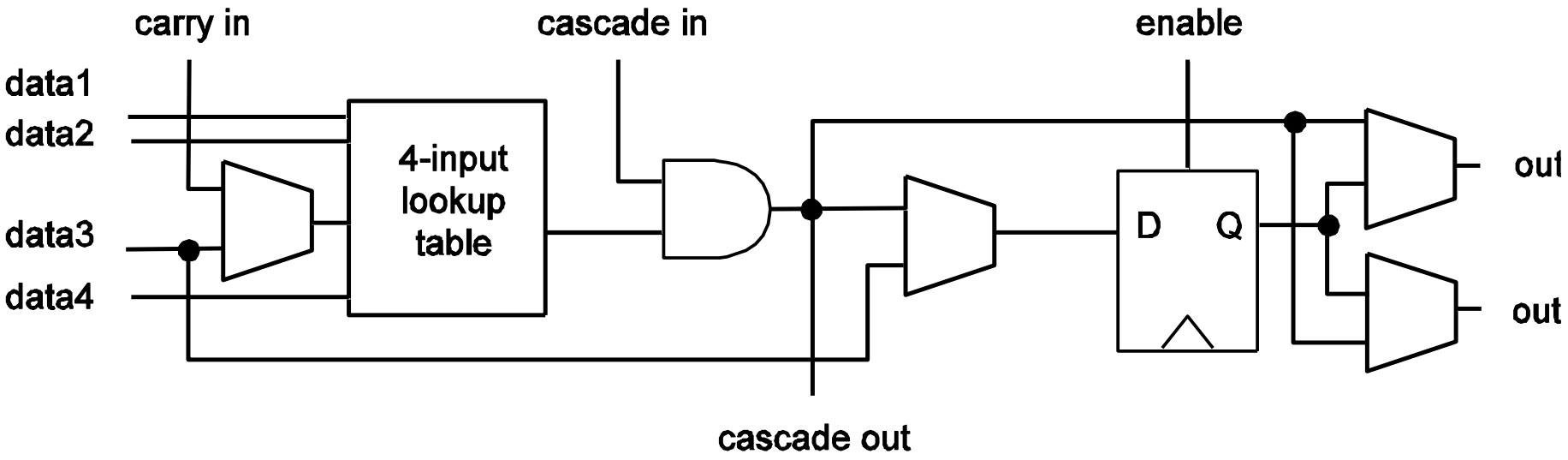
- Each logic array block (LAB) has 10 logic elements.
- Each LE contains LUT, FF.
- Logic elements share some logic – carry and control signal generation


carry in
cascade in
load
clear
data1
data2
data3
data4
lookup table
carry chain
cascade chain
synchronous load/clear logic
D
Q
labclr1
labclr2
chip reset
asynchronous clear/preset/ load logic
labclk1
labclk2
labclkena1
labclkena2

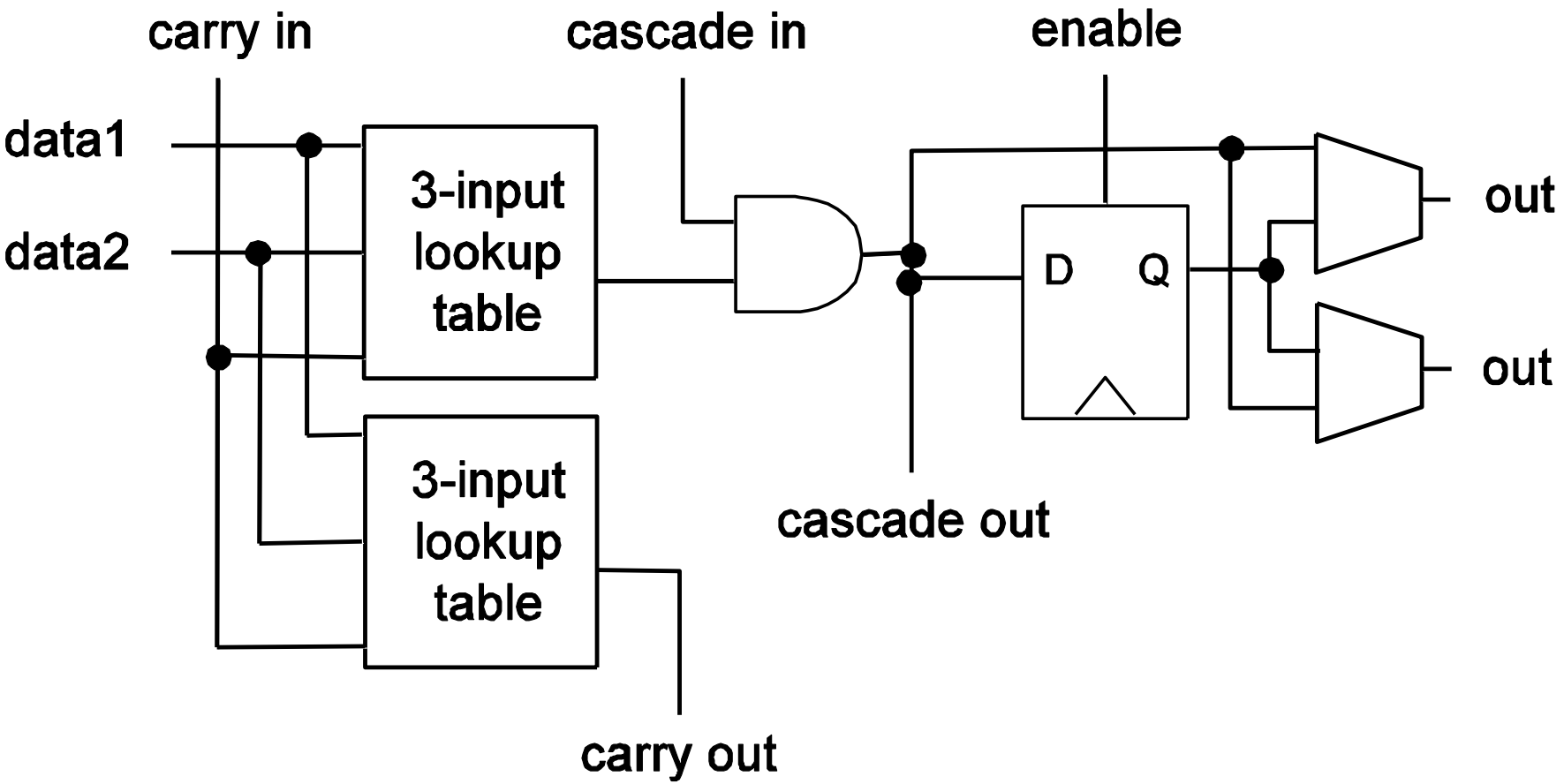
Apex II LE modes

- Modes of operation:
  - Normal.
  - Arithmetic.
  - Counter.

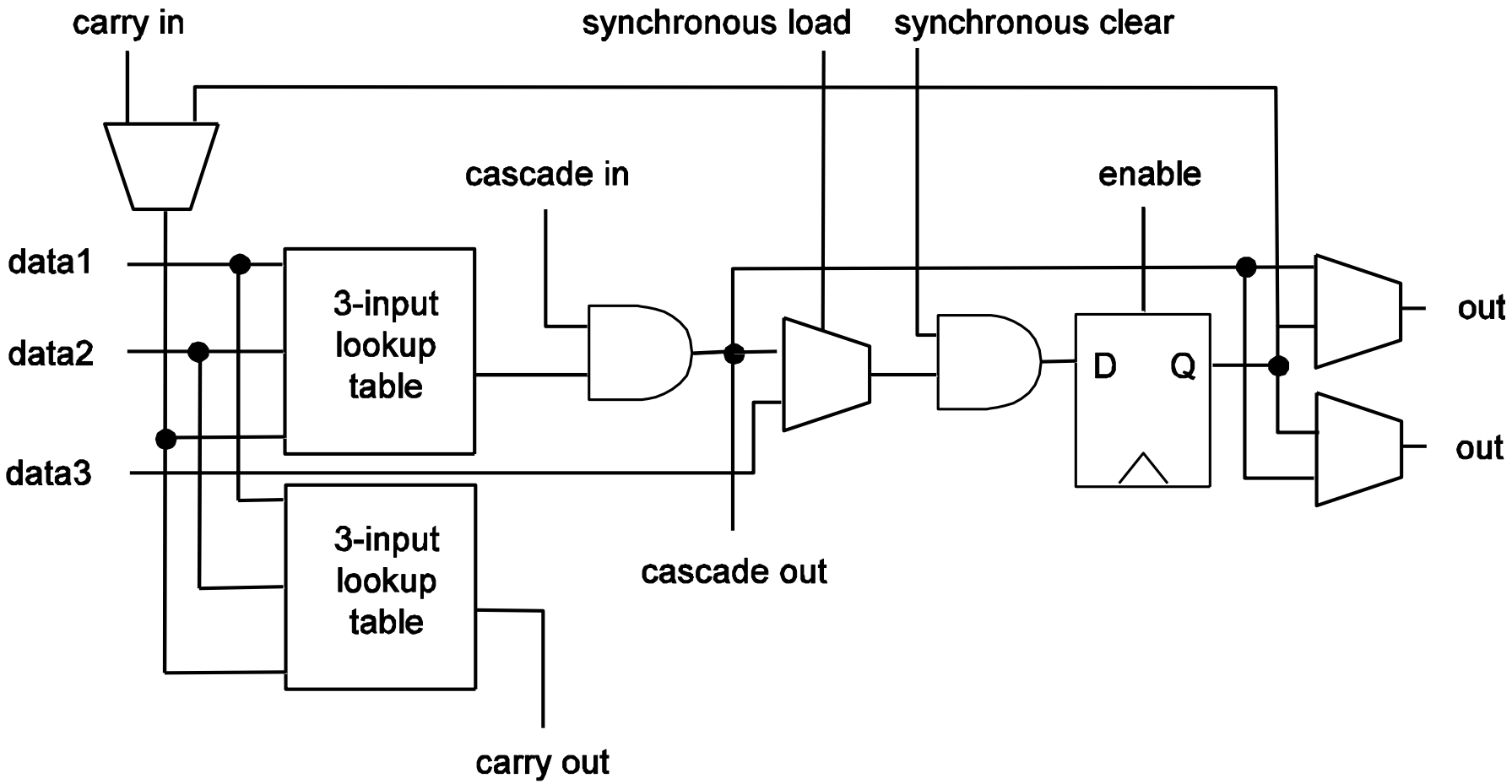
APEX-II LE normal mode



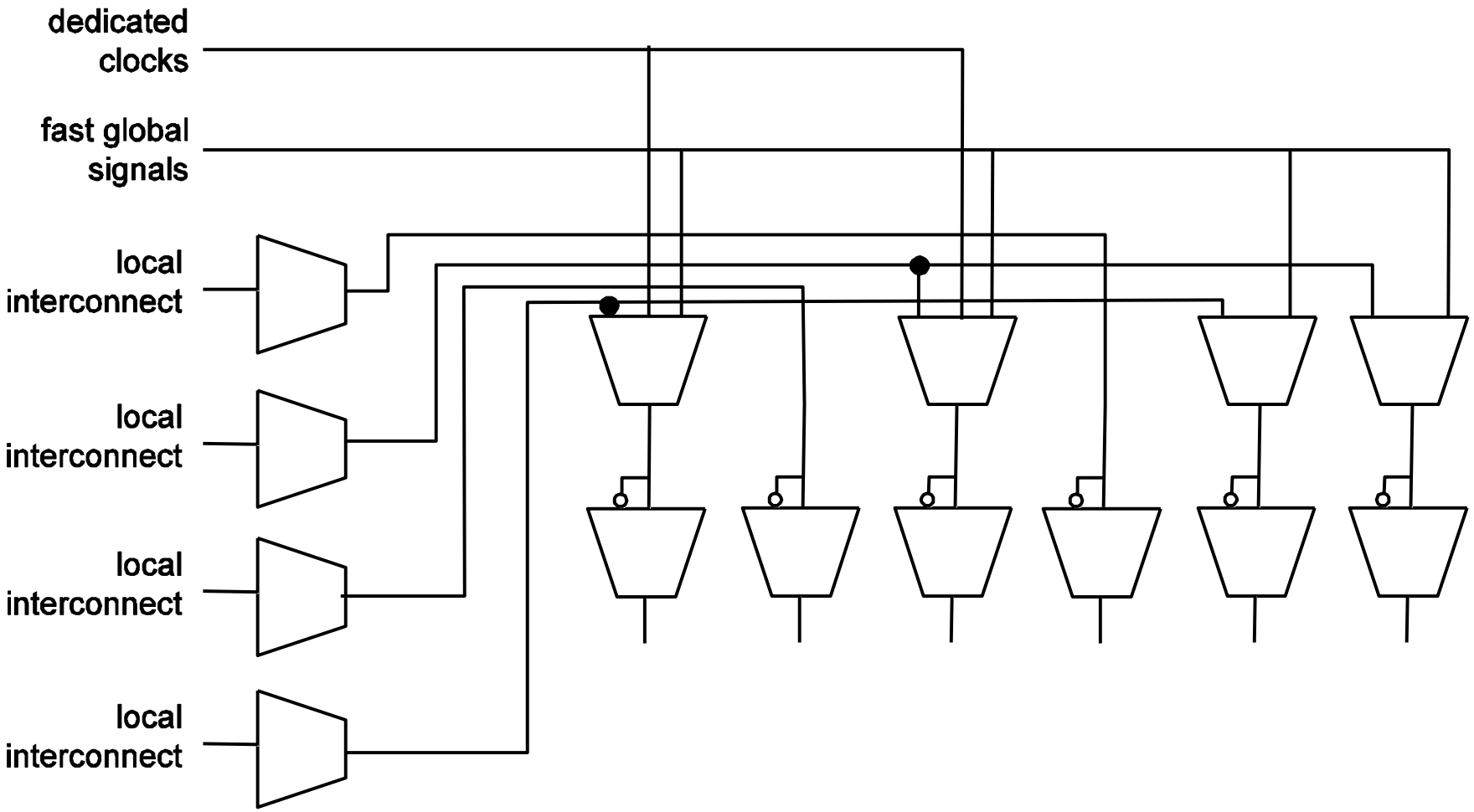
APEX-II LE arithmetic mode



APEX-II LE counter mode

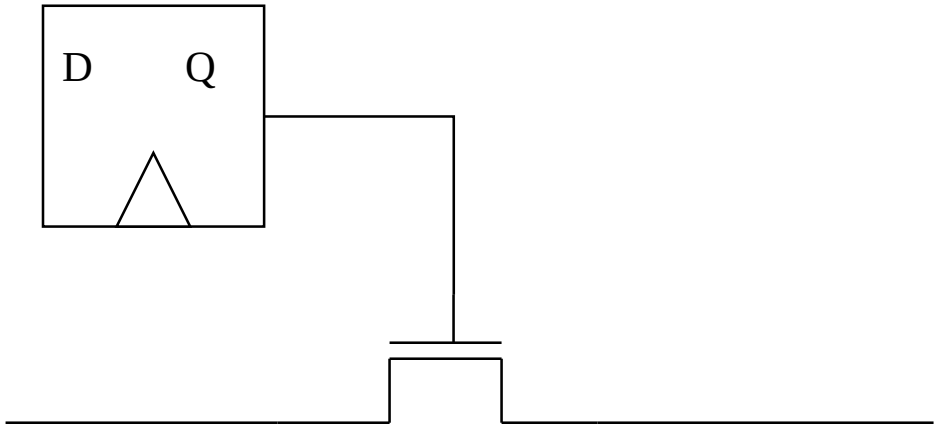


APEX-II LE control logic



Programmable interconnect

- Uses SRAM to hold information used to program interconnect
- MOS switch controlled by configuration bit:
- CMOS transistor – pass transistor
- CMOS has good off state



Programmable vs. fixed interconnect

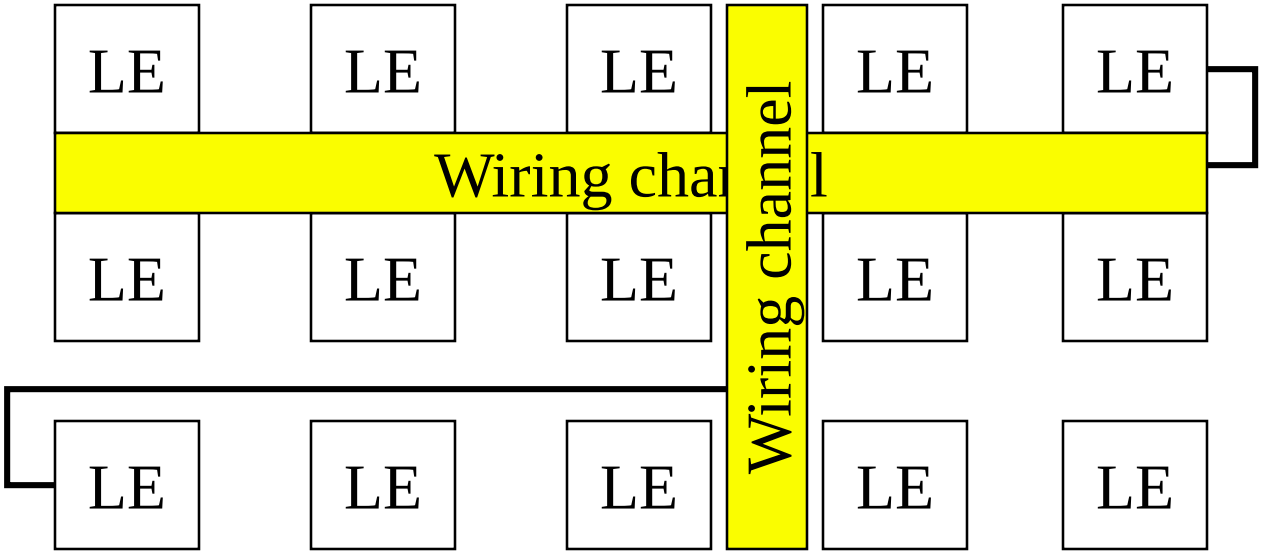
- Switch adds delay.
- Transistor off-state is worse in advanced technologies.
- FPGA interconnect has extra length = added capacitance.

Interconnect strategies

- Some wires will not be utilized.
- Congestion will not be same throughout chip.
- Types of wires:
  - Short wires: local LE connections.
- Global wires: long-distance, buffered communication.
  - Special wires: clocks, etc.

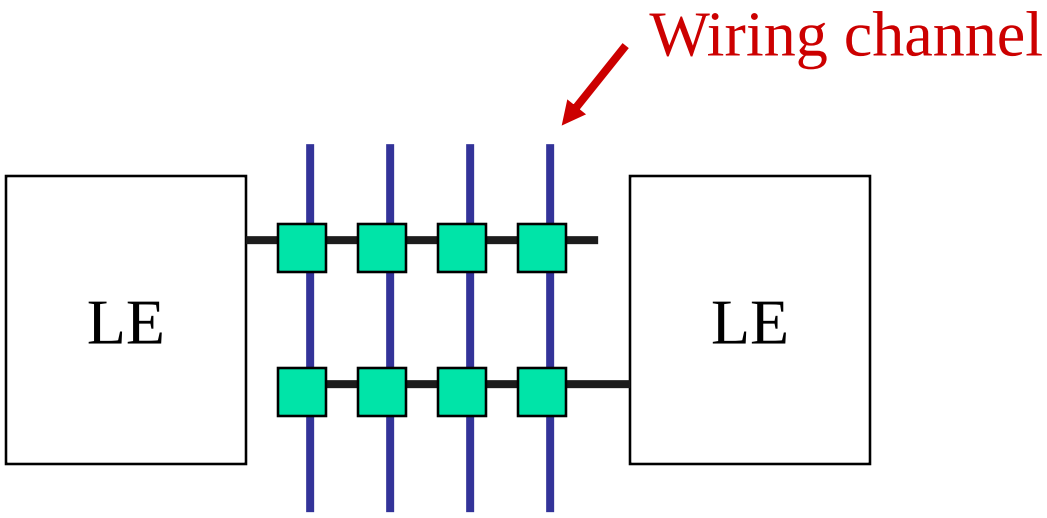
Paths in interconnect

- Connection may be long, complex:



Interconnect architecture

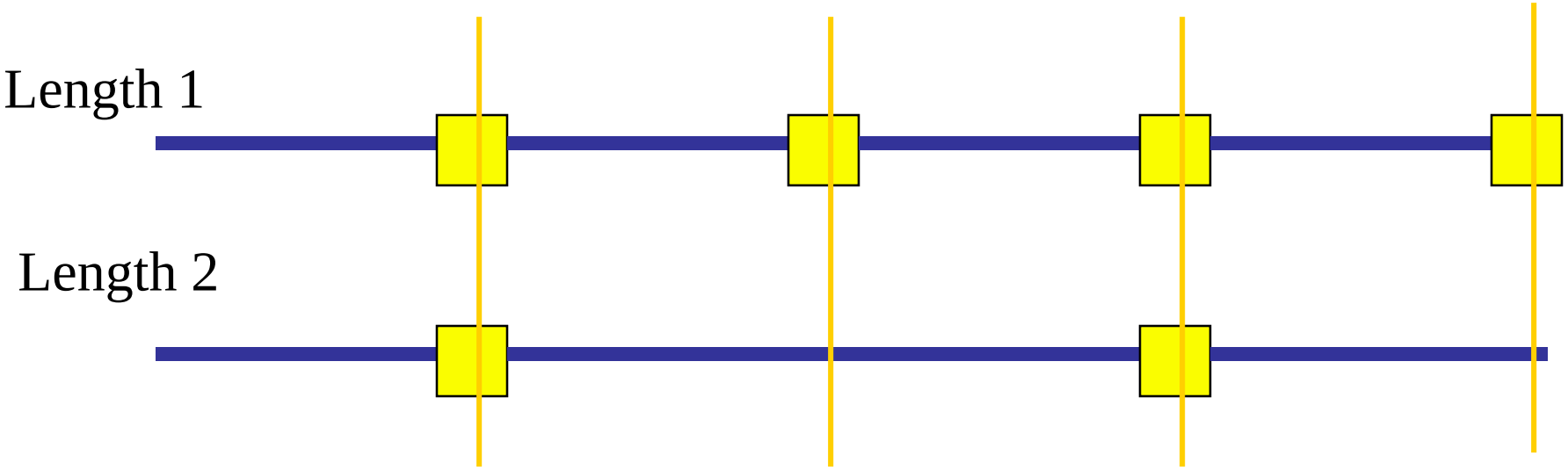
- Connections from wiring channels to LEs.
- Connections between wires in the wiring channels.



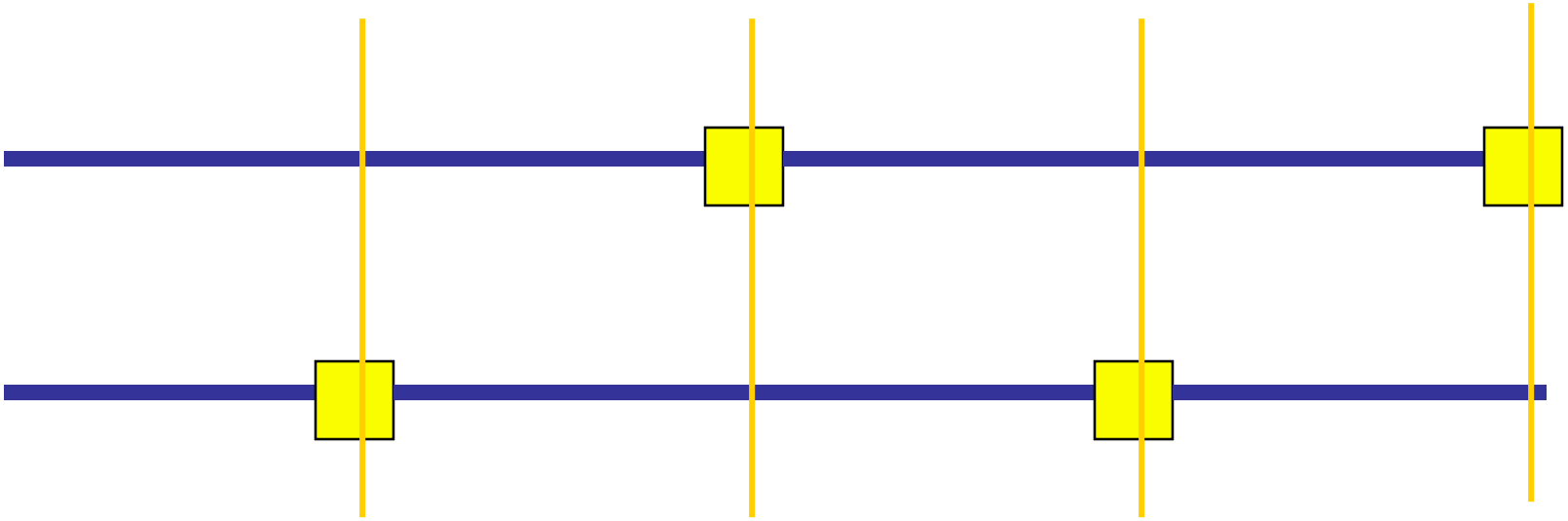
Interconnect richness

- Within a channel:
  - How many wires.
  - Length of segments.
  - Connections from LE to channel.
- Between channels:
  - Number of connections between channels.
  - Channel structure.

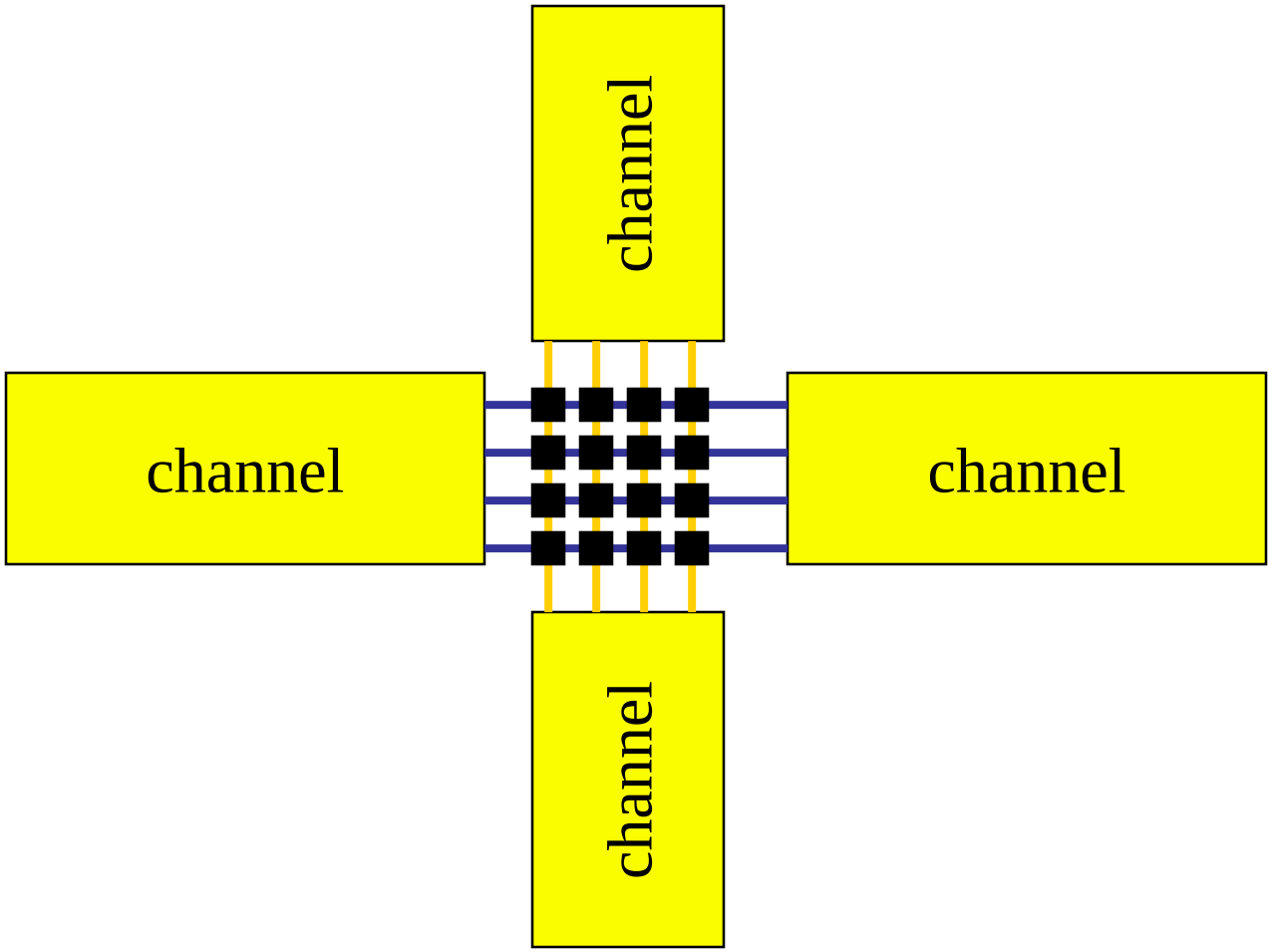
Segmented wiring



Offset segments



Switchbox



Spartan-II interconnect

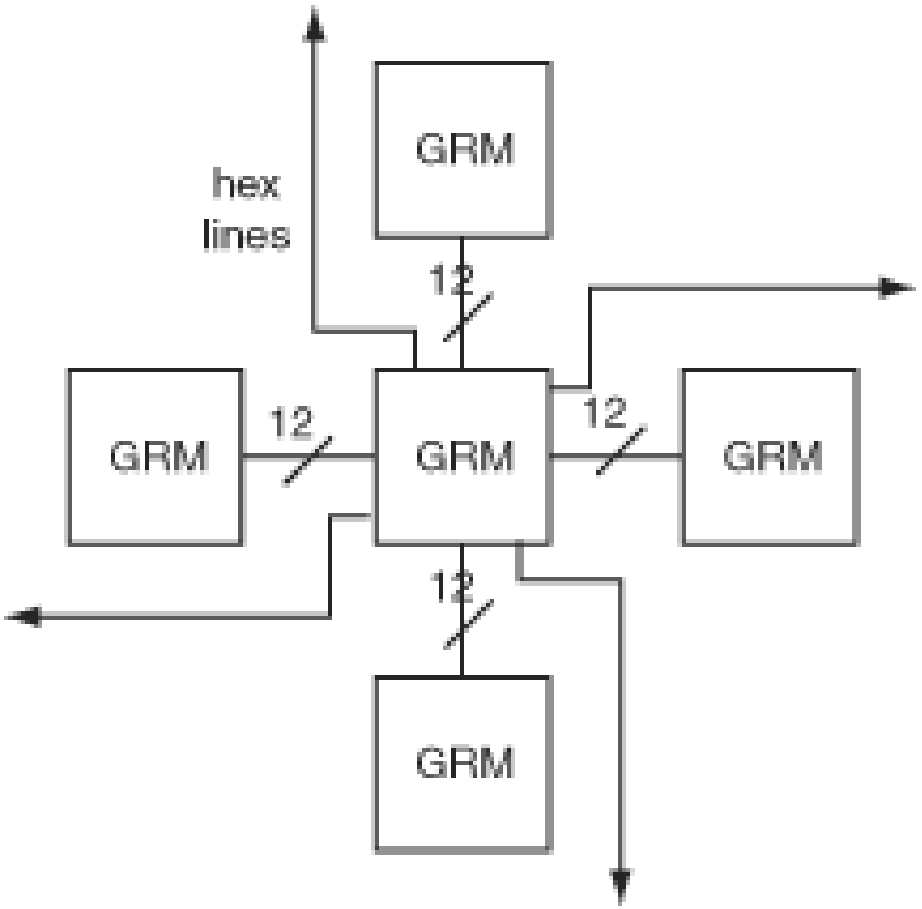
- Types of interconnect:
  - local;
  - general-purpose;
  - dedicated;
  - I/O pin
  - Global
  - Clock

Spartan-II general-purpose network

- Provides majority of routing resources:
  - General routing matrix (GRM) connects horizontal/vertical channels and CLBs.
  - Interconnect between adjacent GRMs.
  - Hex lines connect GRM to GRMs six blocks away.
  - Hex lines provide longer interconnect.
  - 12 longlines span the chip.

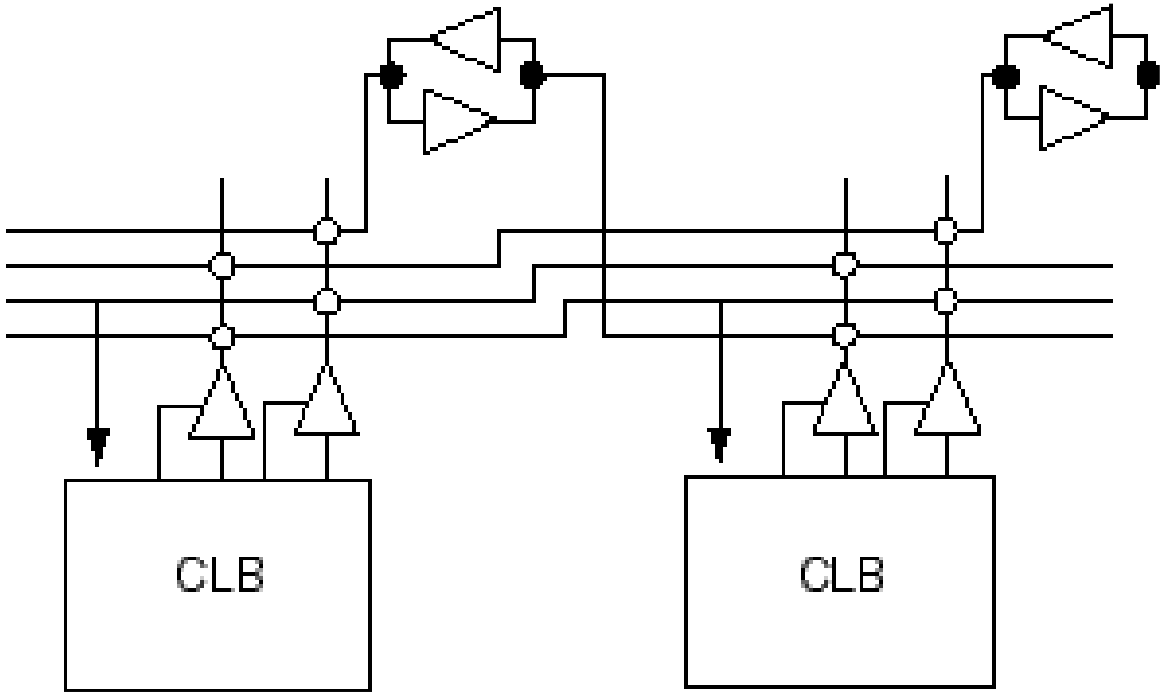
Spartan-II routing

- Relationship between GRM, hex lines, and local interconnect:

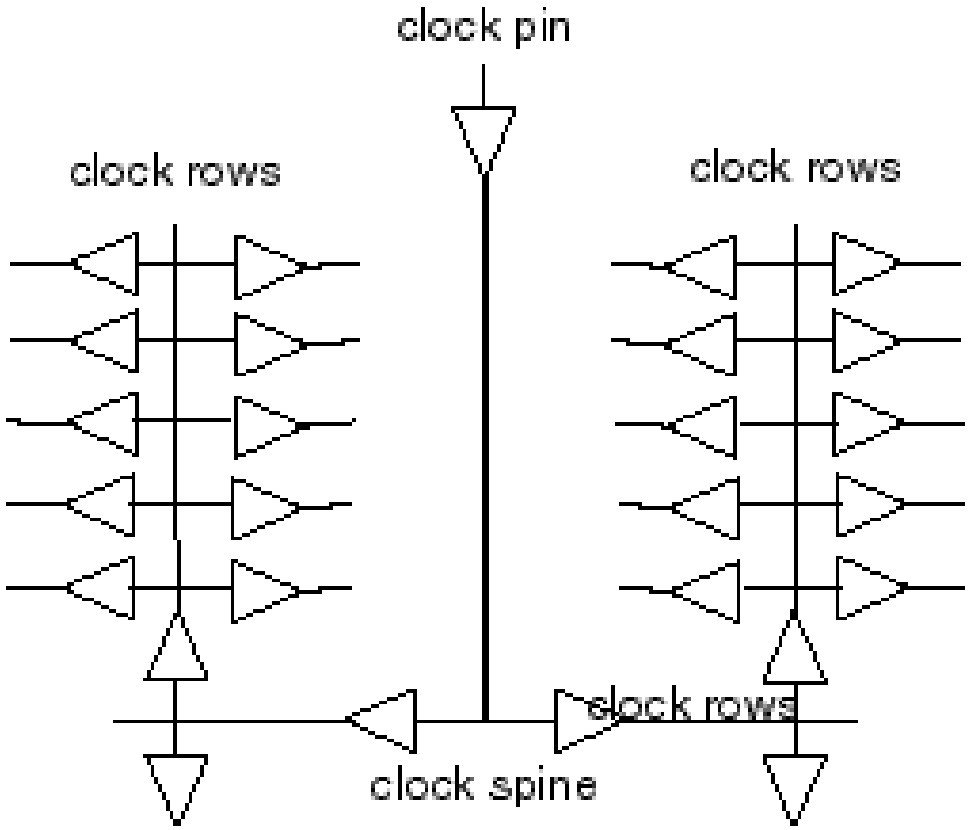


Spartan-II three-state bus

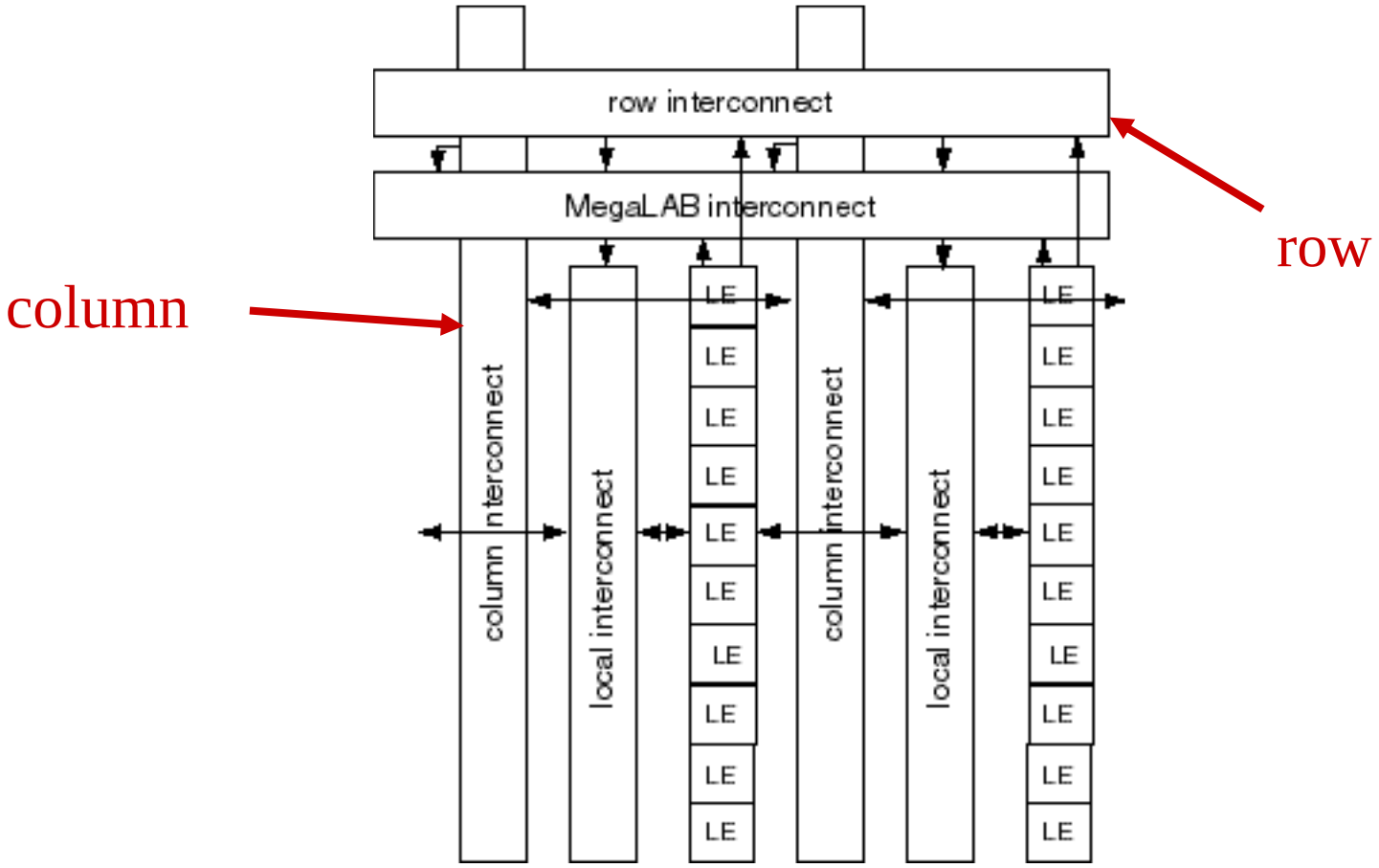
- Horizontal on-chip busses:



Spartan-II clock distribution



Altera APEX II interconnect



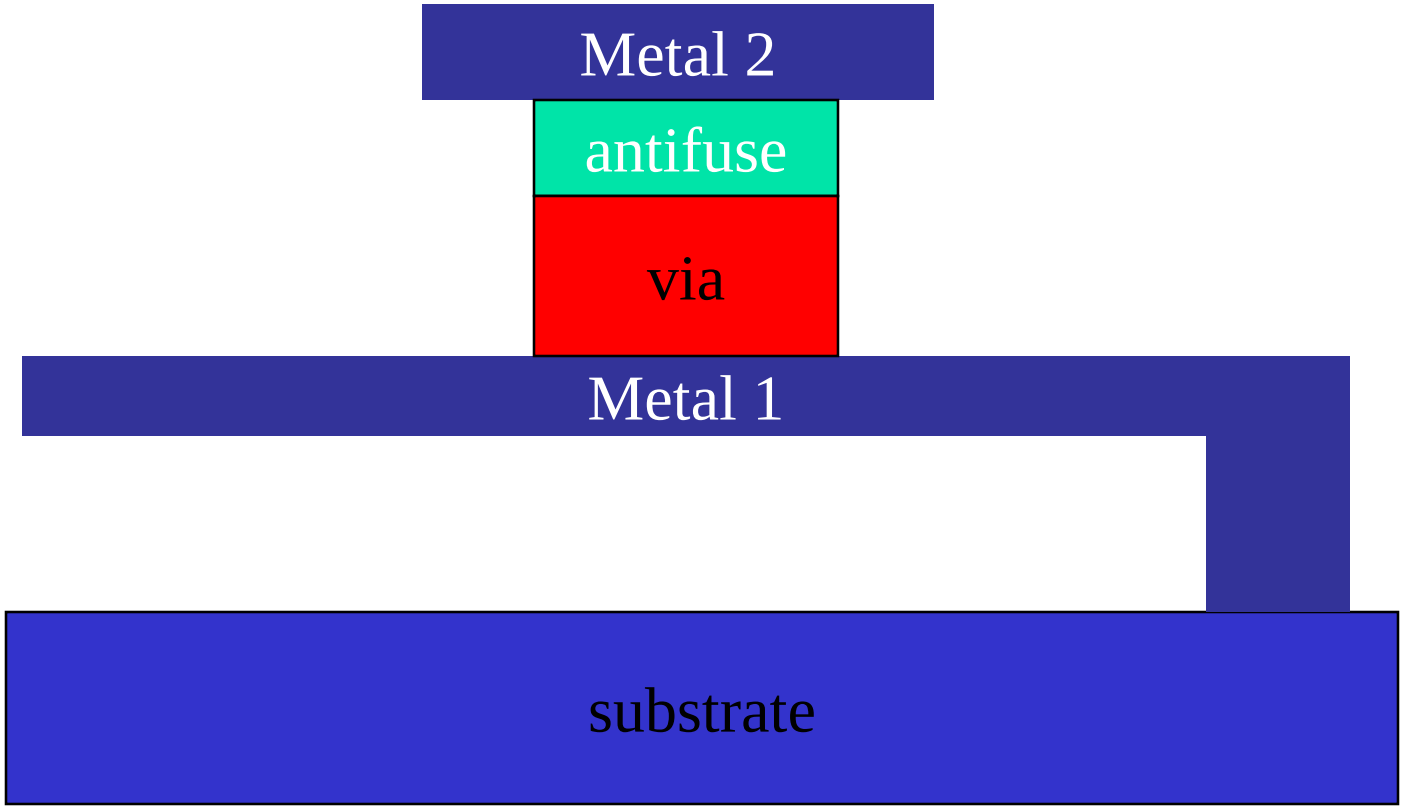
Permanently programmed FPGAs

- Antifuse

Antifuses

- Permanently programmed.
- Make a connection with electrical signal.
- Resistance of about 100 Ω which is more than standard via

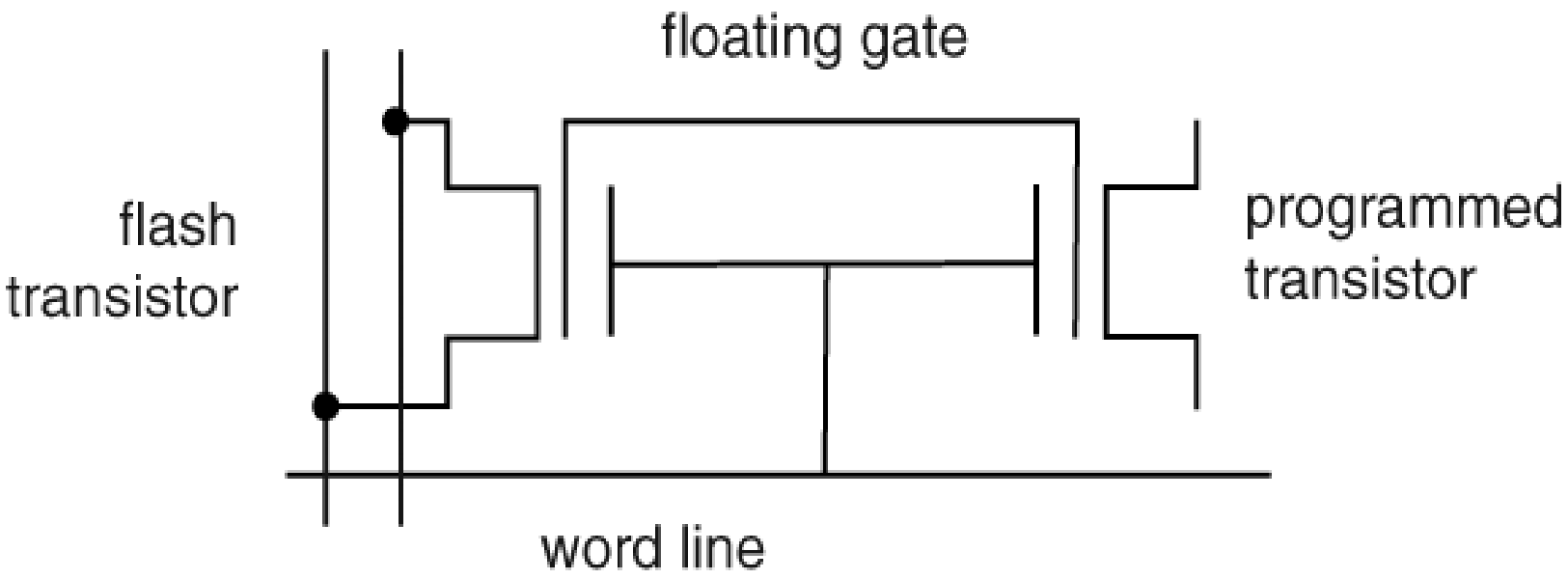
Antifuse structure



Flash-programmed FPGA

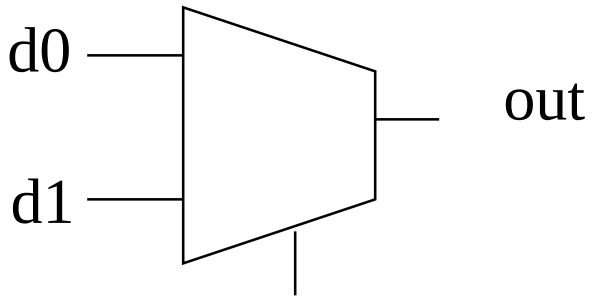
- Flash is high quality programmable read only memory
- Uses a floating gate structure where low leakage capacitor holds a voltage that controls a transistor gate

Flash-programmed switch



Logic blocks

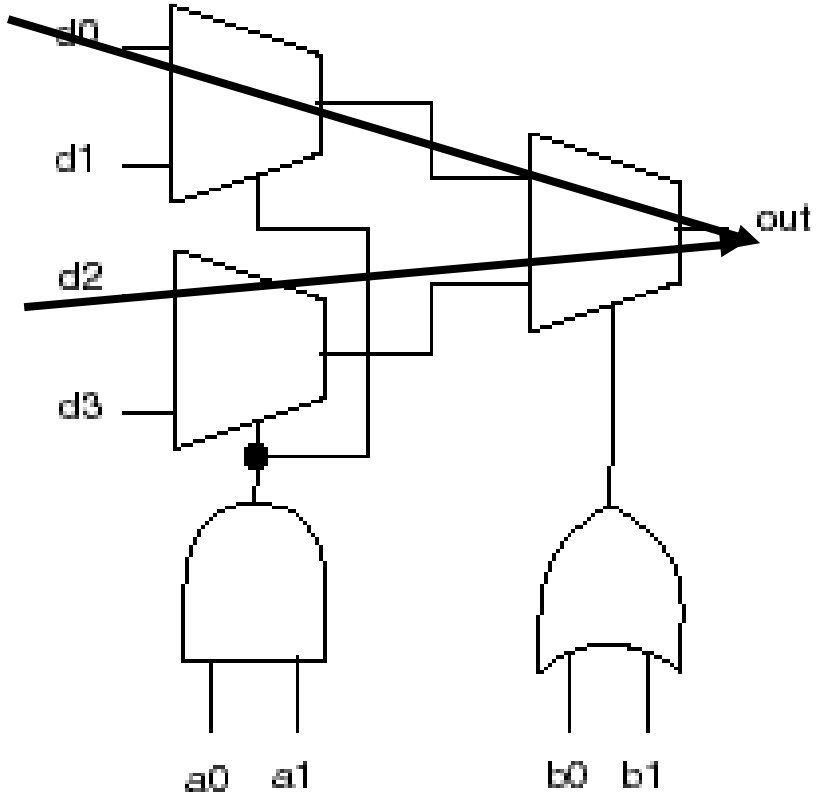
- Program by making connections.
- Based on multiplexing.



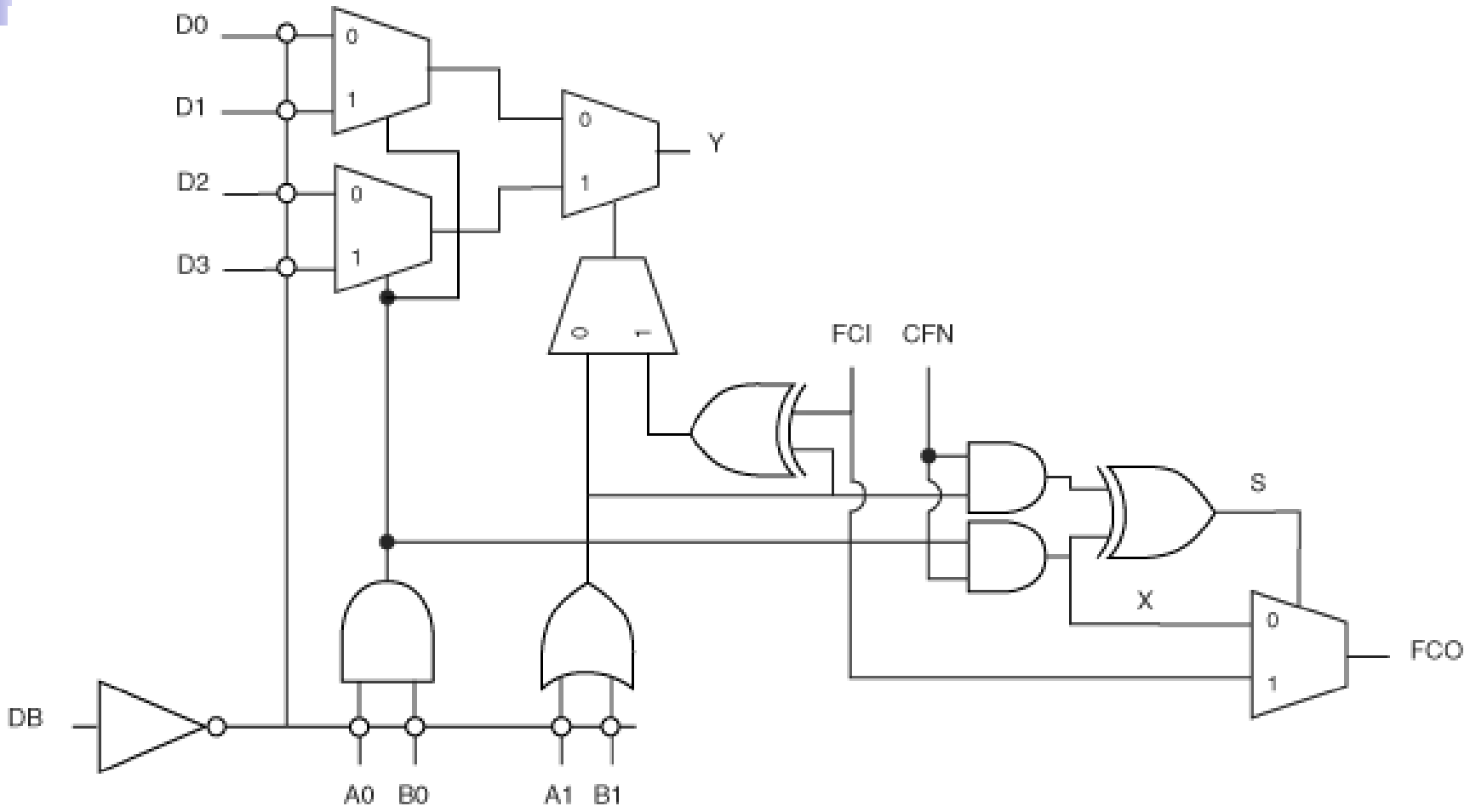
a	out
0	d0
1	d1

Truth table

Larger logic block

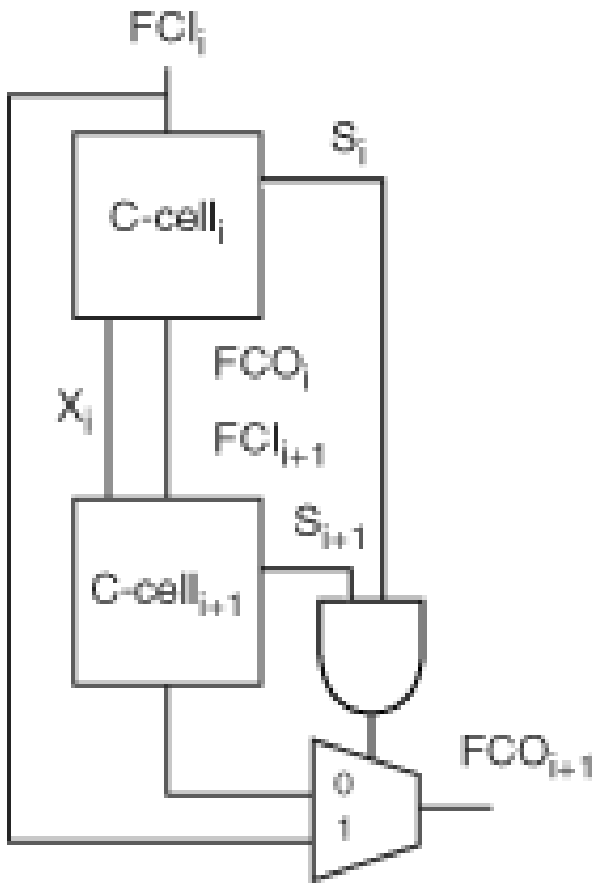


Actel 54SX logic element

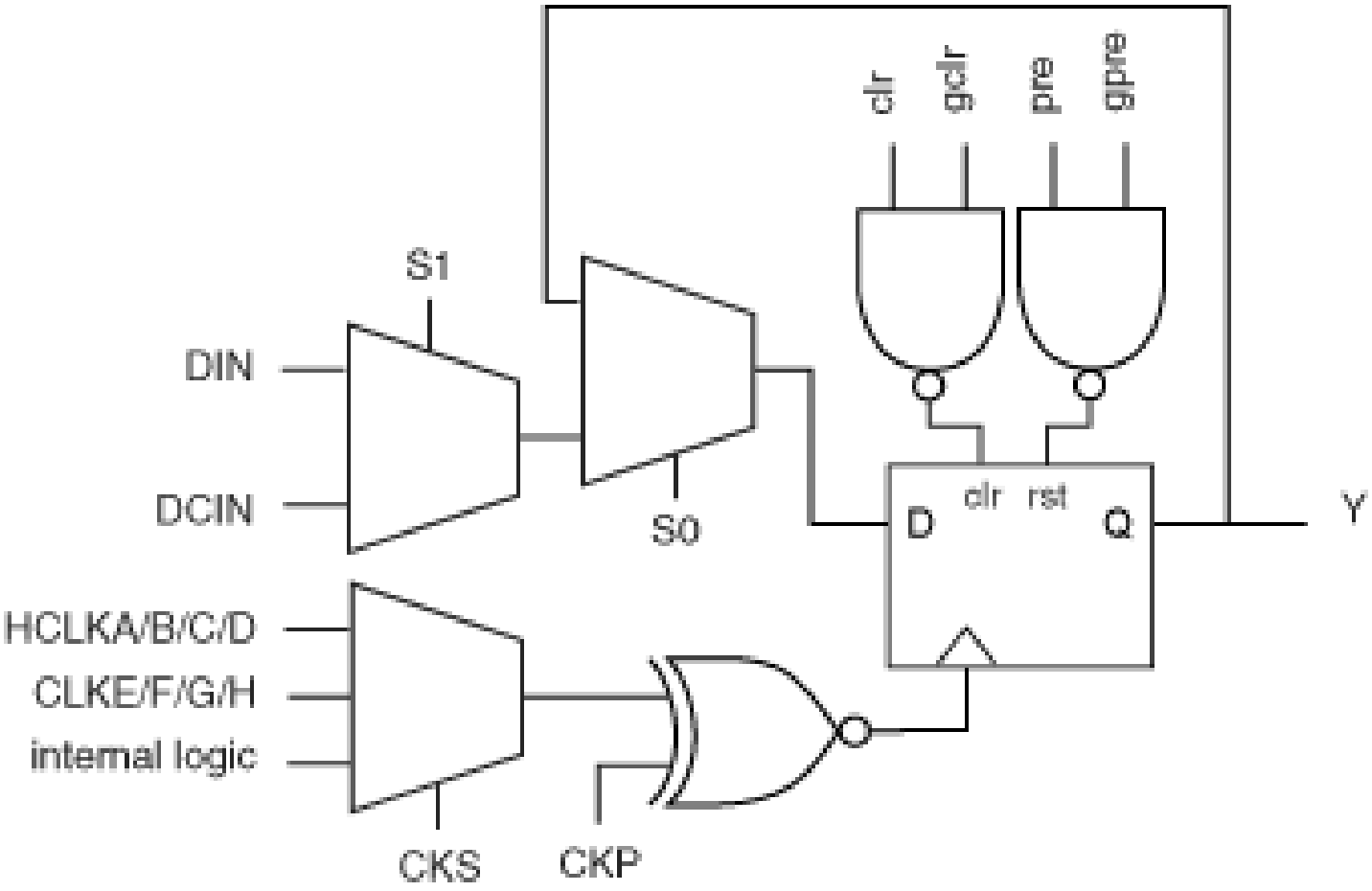


Actel 54SX adder logic

- Uses two C-cells in SuperCluster.
- Adds bits A0 and A1.
- Carry in FCI, carry out FCO.
- Active when CFN is high.



Actel 54SX R cell

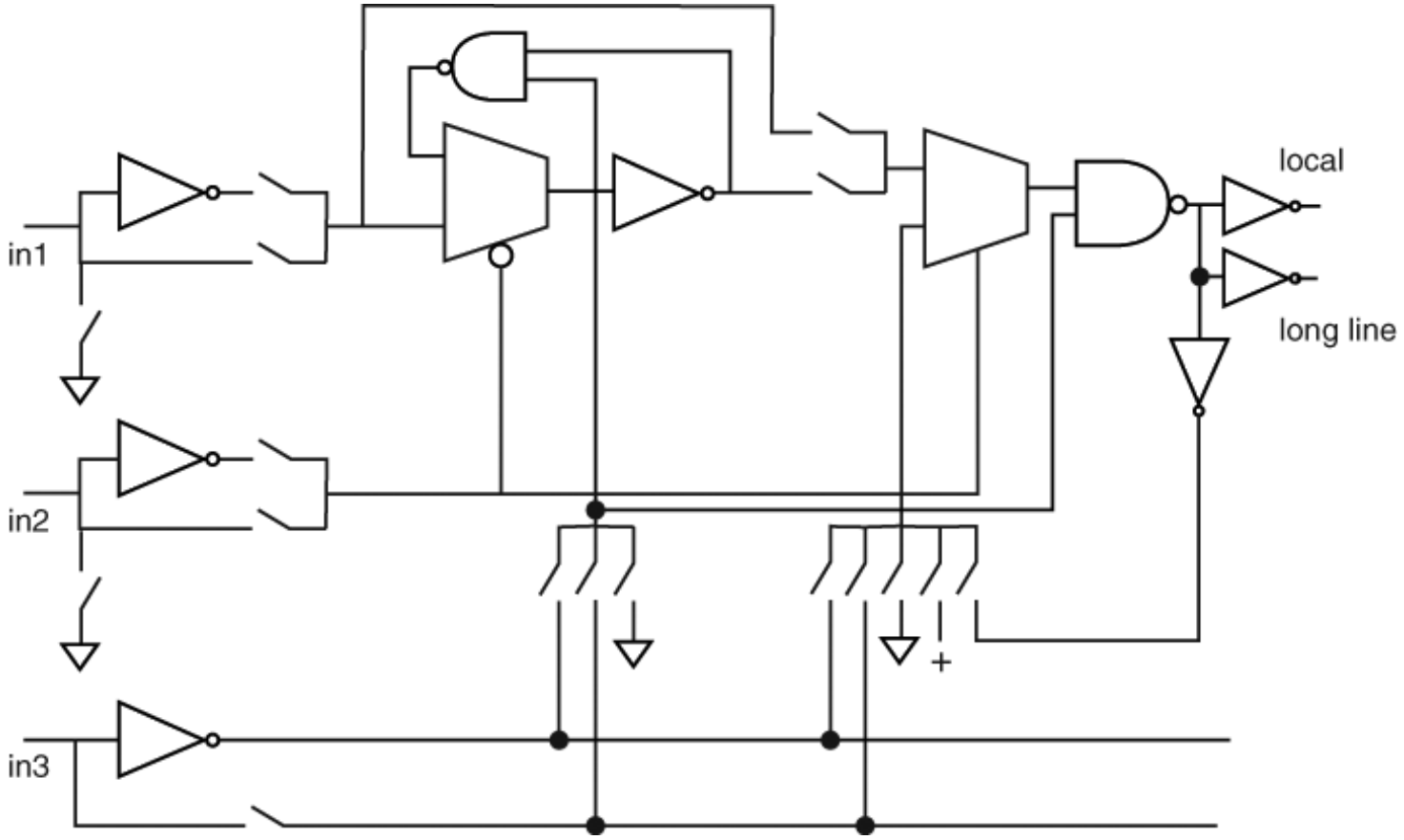


Actel 54SX LE

- C/R cells organized into clusters.
  - Type 1 cluster: CRC.
  - Type 2 cluster: CRR.
- Clusters grouped into superclusters.
  - Type 1: two type 1 clusters.
  - Type 2: one type 1, one type 2.

Actel ProASIC 500K logic gate

- Uses switches to connect inputs, feedback, etc.



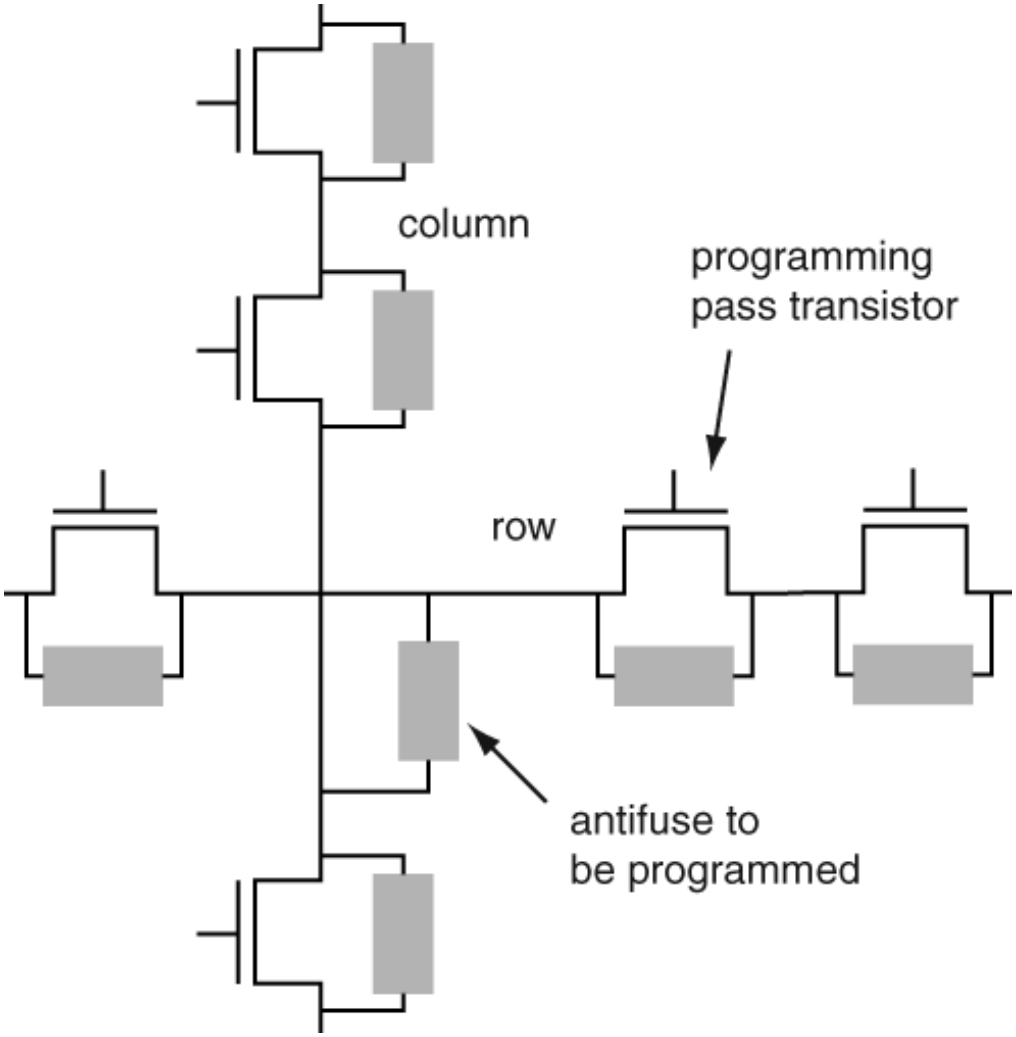
Actel 54SX interconnect

- FastConnect provides horizontal connections between logic modules.
  - Within a supercluster.
  - To supercluster below.
- DirectConnect is within a supercluster:
  - connects C-cell to R-cell neighbor.
- Generic global wiring in segmented channels.

Antifuse programming

- Need to be able to apply programming voltage to every antifuse.
  - Path from VDD to GND.
- Programming can be performed slowly.
  - Don’t need a lot of parallelism.
- Use the wiring network to gain access to the antifuses.
  - Access transistors control path to antifuse.

Antifuse programming access transistors



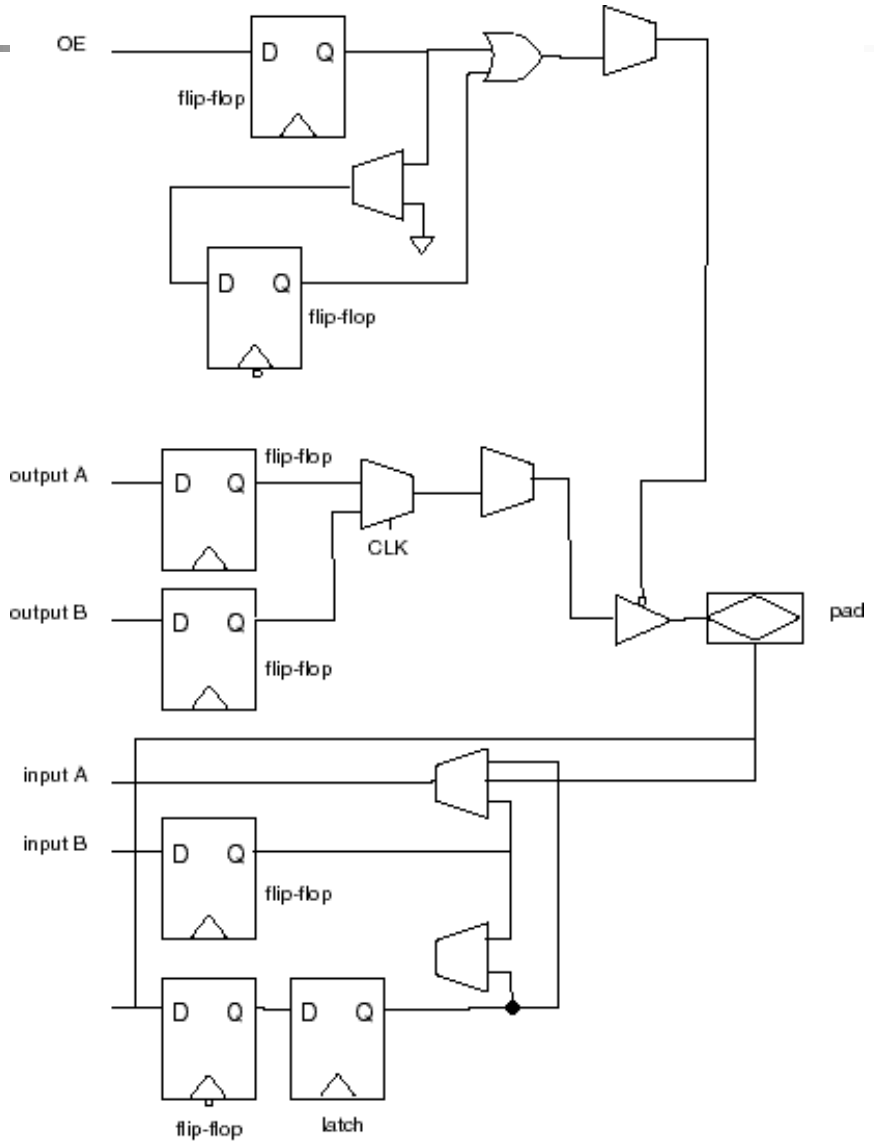
I/O pins

- Need programmable pins:
  - Input or output.
  - Three-state.
- Other features:
  - Registers.
  - Slew rate.
  - Voltage levels.
  - Double-data rate (DDR) support.

Actel APEX II I/O

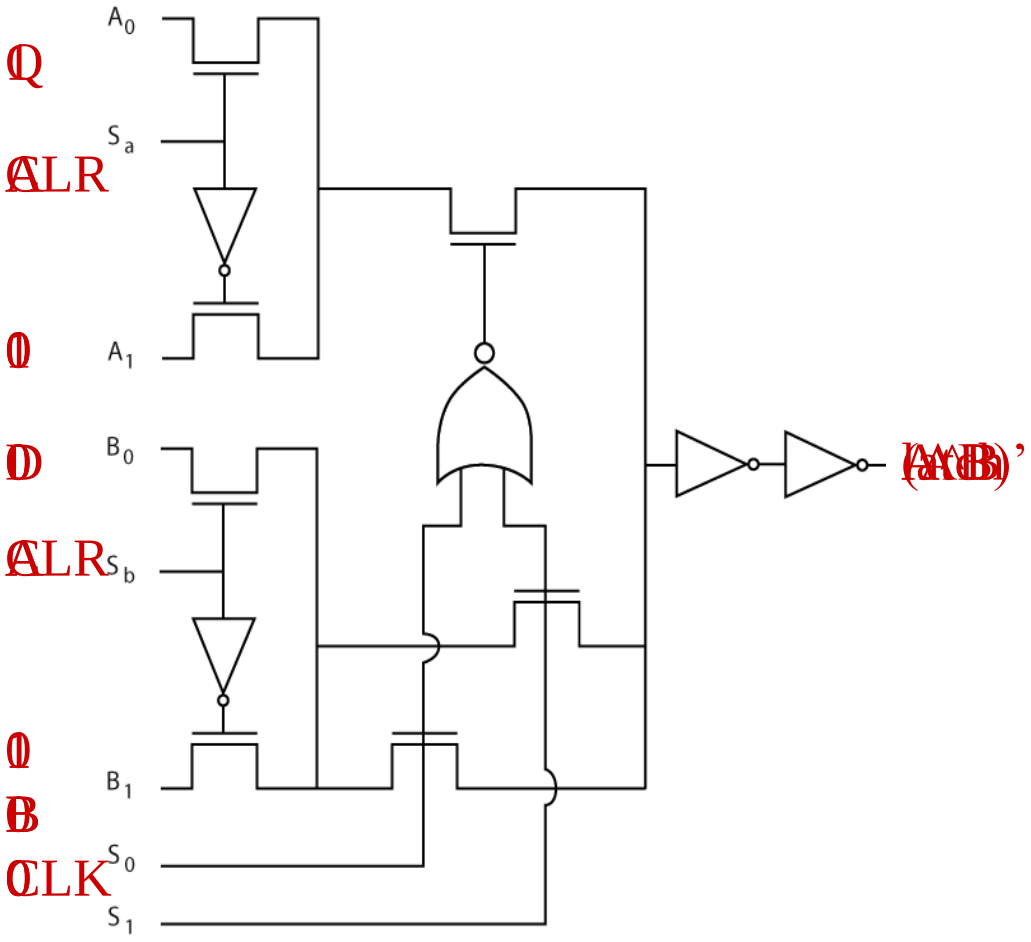
- Supports SDRAM and double-data rate (DDR) memory.
- Six registers and latch.
- Bidirectional buffers.
- Two inputs and two outputs.

APEX II I/O

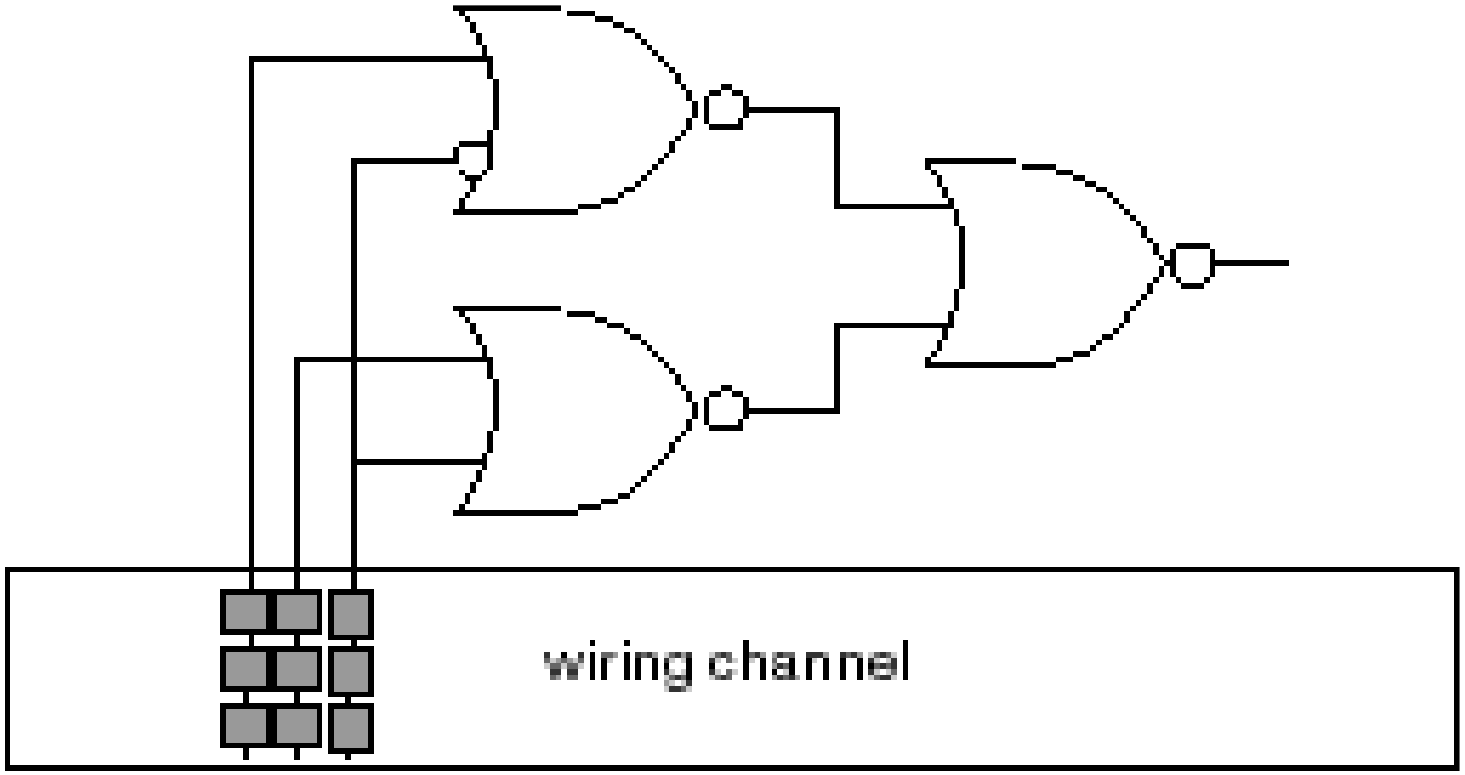

OE
D Q
flip-flop
D Q
flip-flop
output A
D Q
flip-flop
CLK
output B
D Q
flip-flop
pad
input A
input B
D Q
flip-flop
D Q
D Q
flip-flop
latch

- Circuit design for FPGAs:
- Logic elements.
  - Interconnect.

Multiplexers as logic elements



Using antifuses

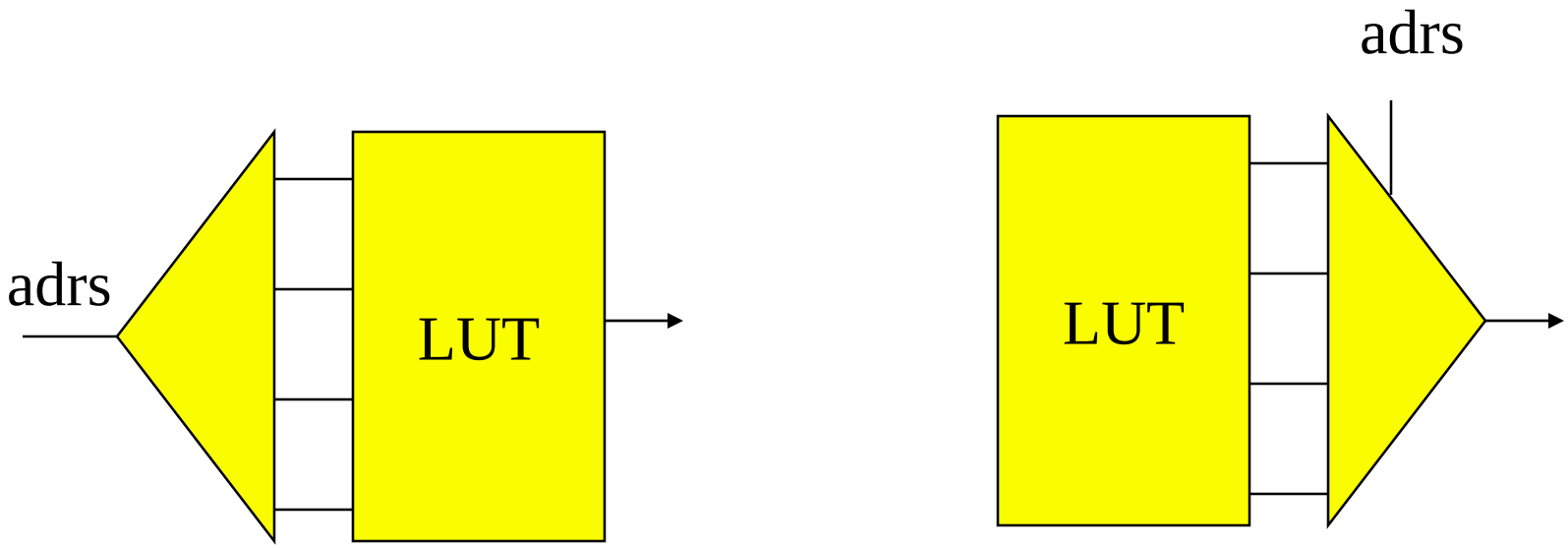


Static CMOS gate vs. LUT

- Number of transistors:
  - NAND/NOR gate has 2n transistors.
  - 4-input LUT has 128 transistors in SRAM, 96 in multiplexer.
- Delay:
  - 4-input NAND gate has 9τ delay.
  - SRAM decoding has 21τ delay.
- Power:
  - Static gate's power depends on activity.
  - SRAM always burns power.

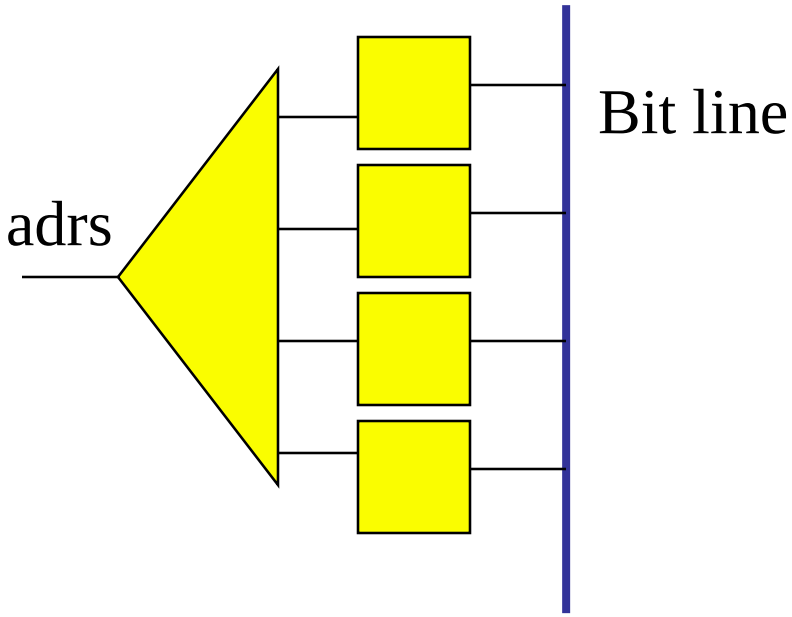
Lookup table circuitry

- Demultiplexer or multiplexer?



Traditional RAM/ROM

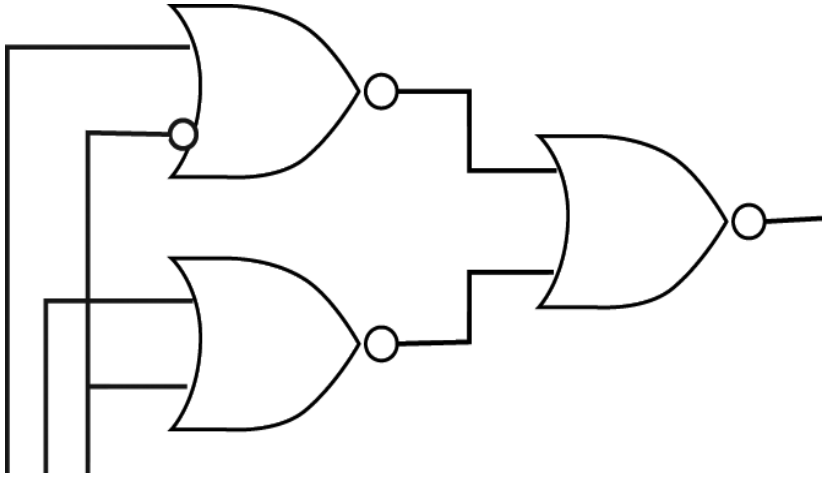
- Cell drives long bit line:



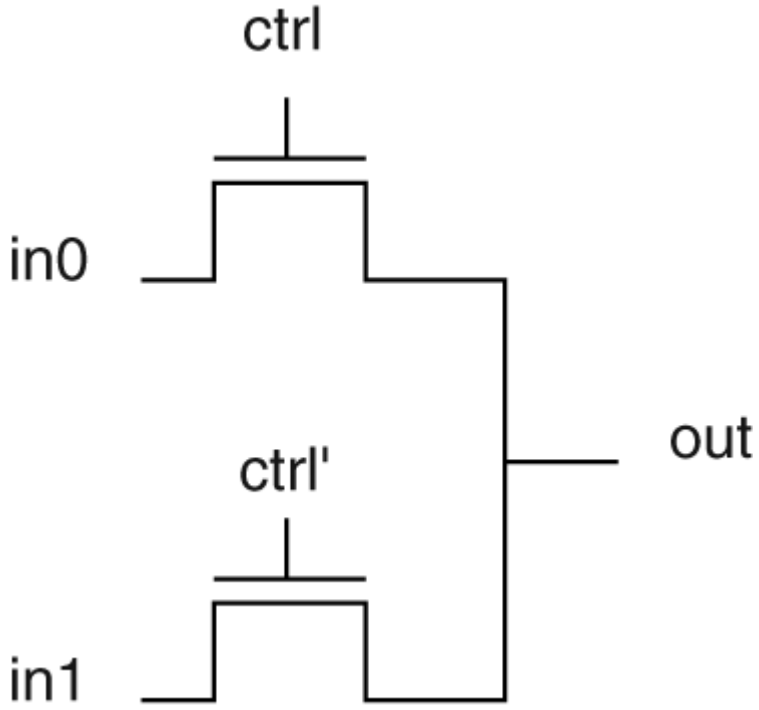
Lookup memory

- Multiplexer presents smaller load to memory cells.
  - Allows smaller memory cells.

Multiplexer styles



static gates



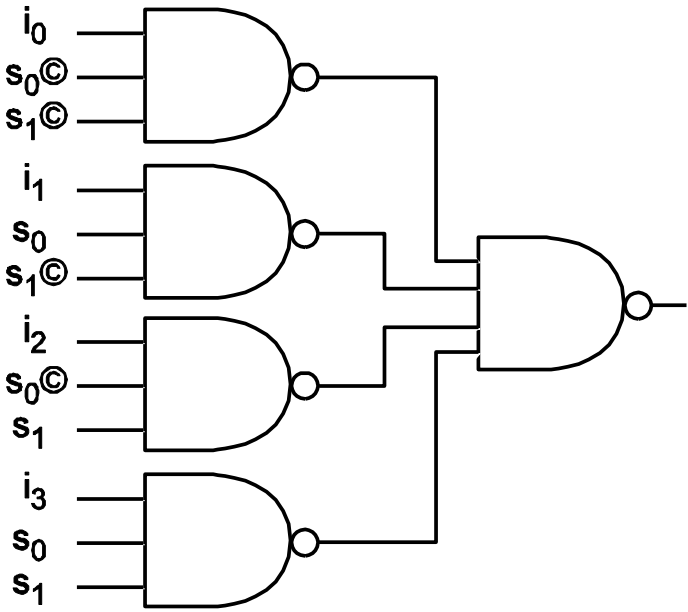
pass transistors

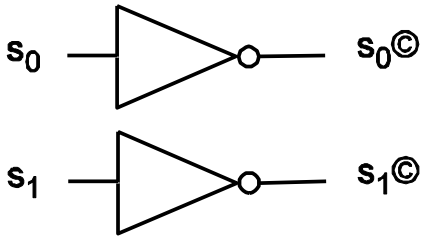
Multiplexer design

- Pass transistor multiplexer uses fewer transistors than fully complementary gates.
- Pass transistor is somewhat faster than complementary switch:
  - Equal-strength p-type is 2.5X n-type width.
  - Total resistance is 0.5X, total capacitance is 3.5X.
  - RC delay is 0.5 x 3.5 = 1.75 times n-type switch.

Static gate four-input mux

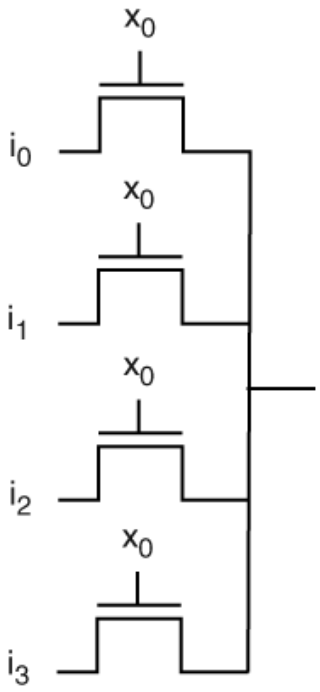
- Delay through n-input NAND is (n+2)/3.
- Lg b + 1 inputs at first level, so delay is (lg b + 3)/3.
- Delay at second level is (b+2)/3.
- Delay grows as b lg b.

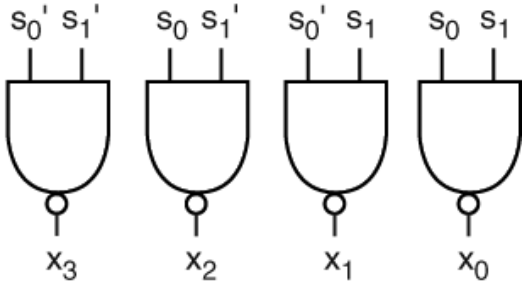




Pass-transistor-based four-input mux

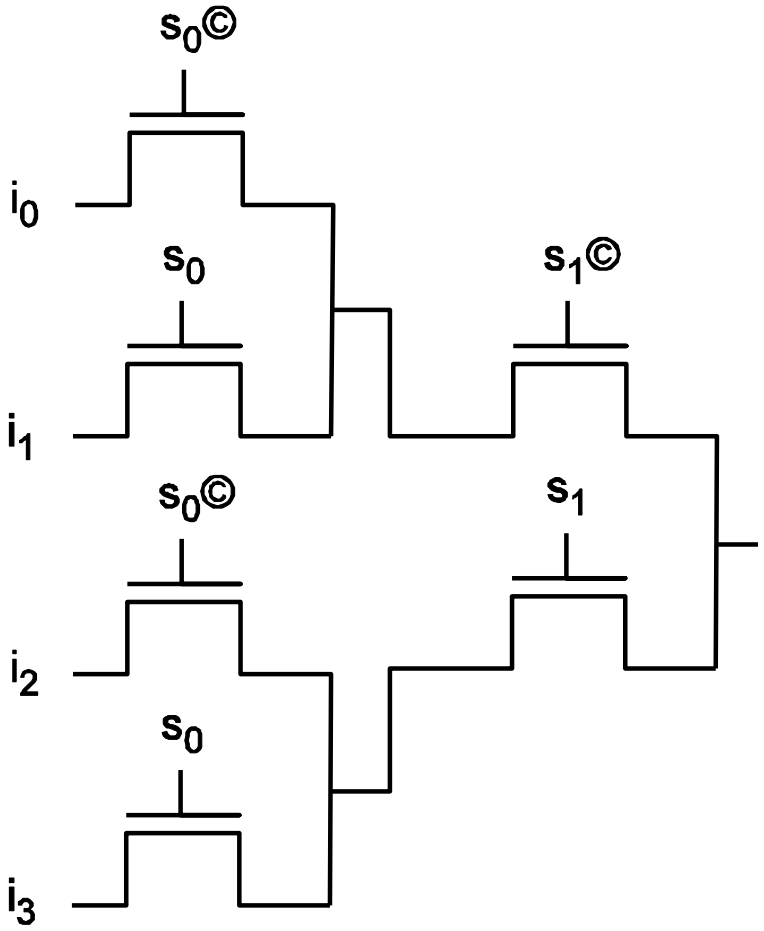
- Must include decode logic in total delay.





Tree-based four-input mux

- Delay proportional to square of path length.
- Delay grows as lg b^2.

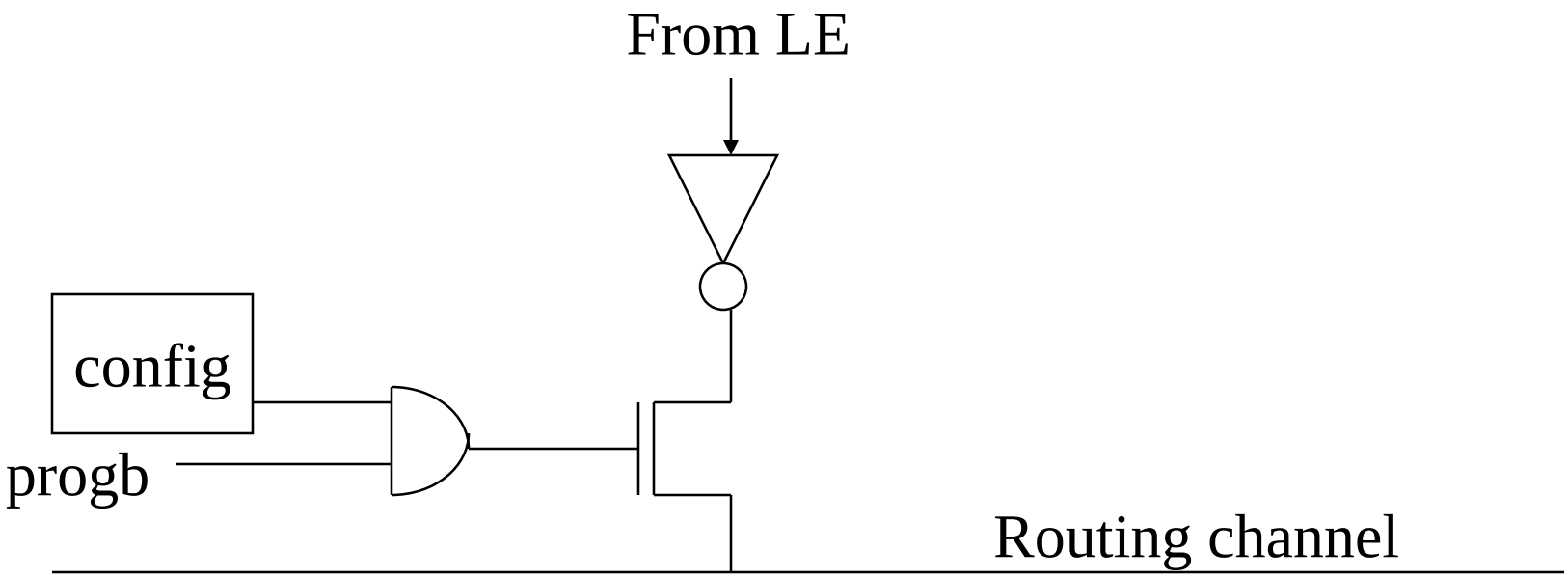


LE output drivers

- Must drive load:
  - Wire;
  - Destination LE.
- Different types of wiring present different loads.

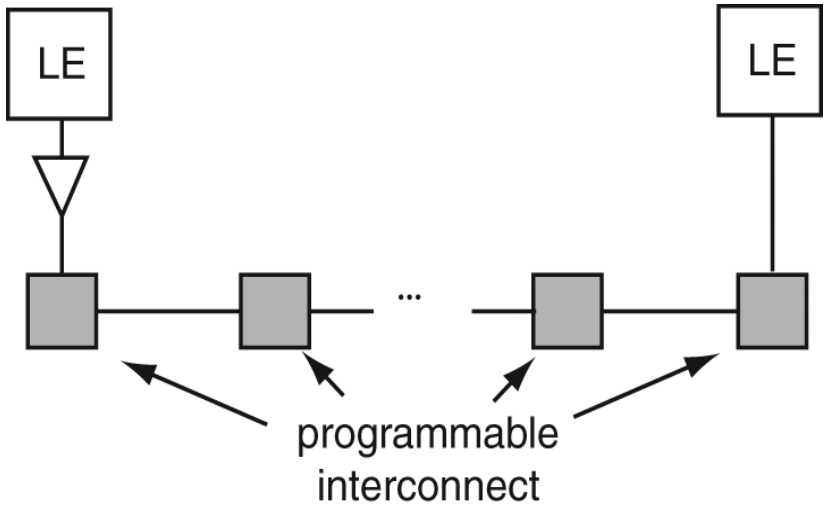
Avoiding programming hazards

- Want to disable connections to routing channel before programming.



Interconnect circuits

- Why so many types of interconnect?
  - Provide a choice of delay alternatives.
- Sources of delay:
  - Wires.
  - Programming points.



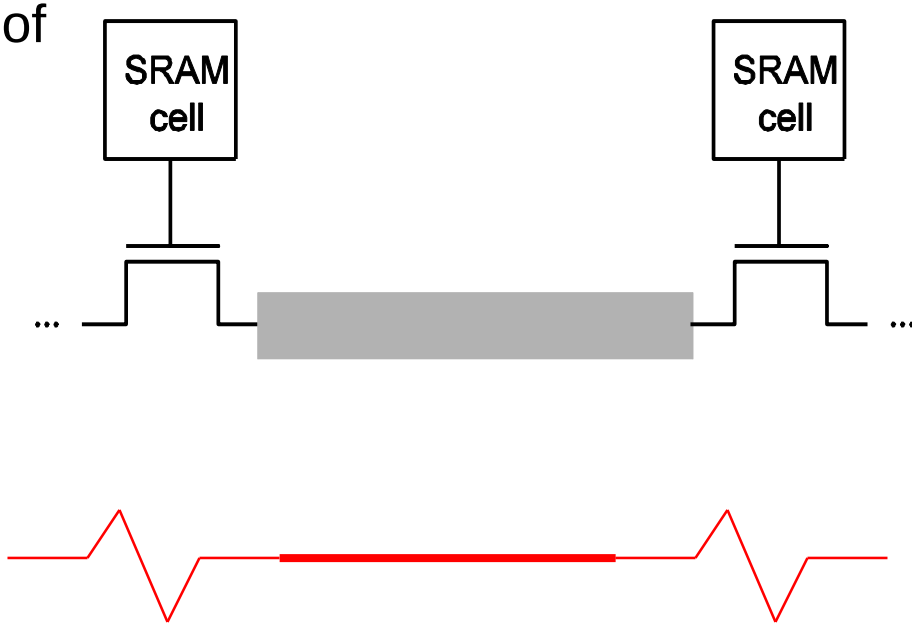
Styles of programmable interconnection point

pass transistor

Three-state

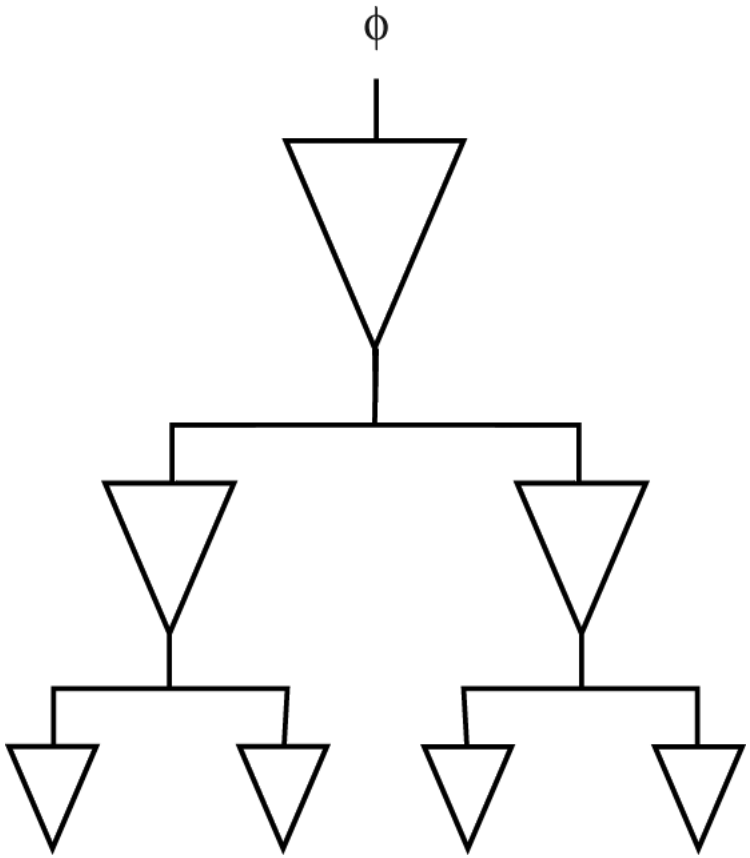
Pass transistor programmable interconnect point

- Small area.
- Resistive switch.
- Delay grows as the square of the number of switches.



Clock drivers

- Clock driver tree:



Clock nets

- Must drive all LEs.
- Design parameters:
  - number of fanouts;
  - load per fanout;
  - wiring tree capacitance.
- Determine optimal buffer sizes.