Switch Level Modeling

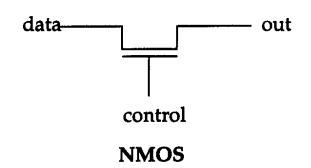


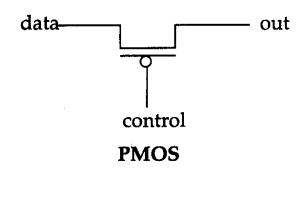
Switch modeling elements

- MOS switches
 - nmos
 - pmos
- nmos (out, data, control)
- pmos (out, data, control)

| | | control | | | | |
|------|---|---------|---|---|---|--|
| nmos | | 0 | 1 | x | Z | |
| data | 0 | Z | 0 | L | L | |
| | 1 | Z | 1 | Н | Н | |
| | x | Z | x | x | x | |
| | z | z | Z | z | Z | |
| | | | | | | |

| | | control | | | | |
|------|---|---------|---|---|---|--|
| pmos | | 0 | 1 | X | Z | |
| data | 0 | 0 | Z | L | L | |
| | 1 | 1 | Z | Н | Н | |
| | x | x | Z | x | x | |
| | z | z | z | Z | Z | |
| | | 1 | | | | |

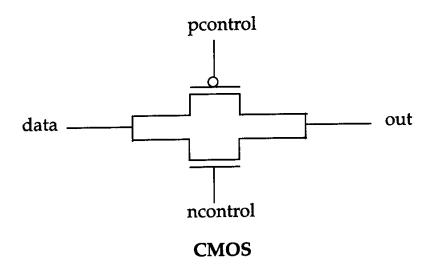






Switch modeling elements

- CMOS switches
 - nmos (out, data, ncontrol, ncontrol)





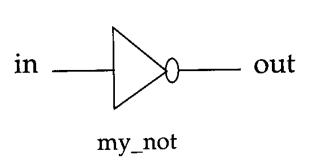
Power and ground

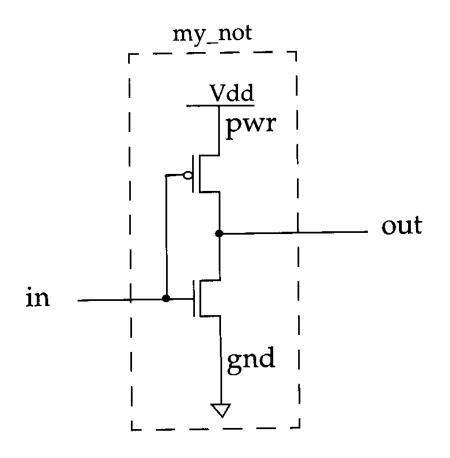
- supply1, supply0

```
supply1 vdd;
supply0 gnd;
assign a = vdd; //Connect a to vdd
assign b = gnd; //Connect b to gnd
```



CMOS inverter



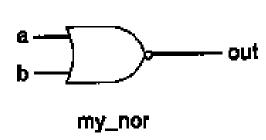


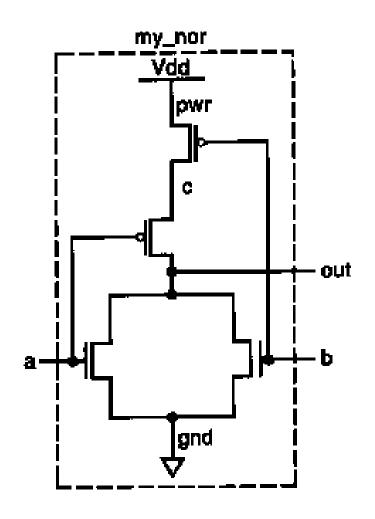


```
//Define an inverter using MOS switches
module my_not(out, in);
output out;
input in;
//declare power and ground
supply1 pwr;
supply0 gnd;
//instantiate nmos and pmos switches
pmos (out, pwr, in);
nmos (out, gnd, in);
endmodule
```



CMOS NOR gate





CMOS NOR gate

```
//Define our own nor gate, my_nor
module my nor(out, a, b);
output out;
input a, b;
//internal wires
wire c:
//set up power and ground lines
supply1 pwr; //pwr is connected to Vdd (power supply)
supply0 gnd; //gnd is connected to Vss(ground)
//instantiate pmos switches
pmos (c, pwr, b);
pmos (out, c, a);
//instantiate nmos switches
nmos (out, gnd, a);
nmos (out, gnd, b);
endmodule
```